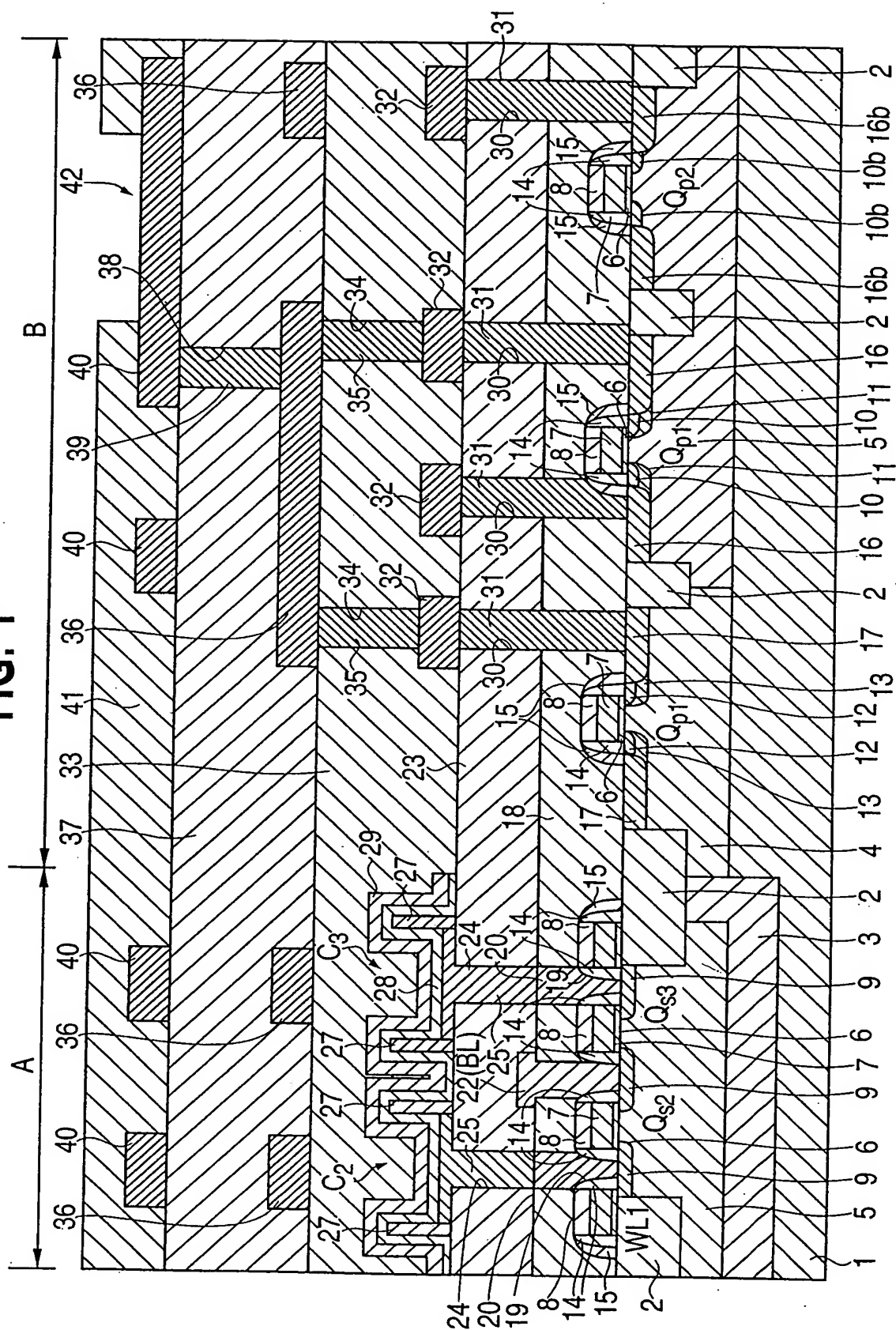
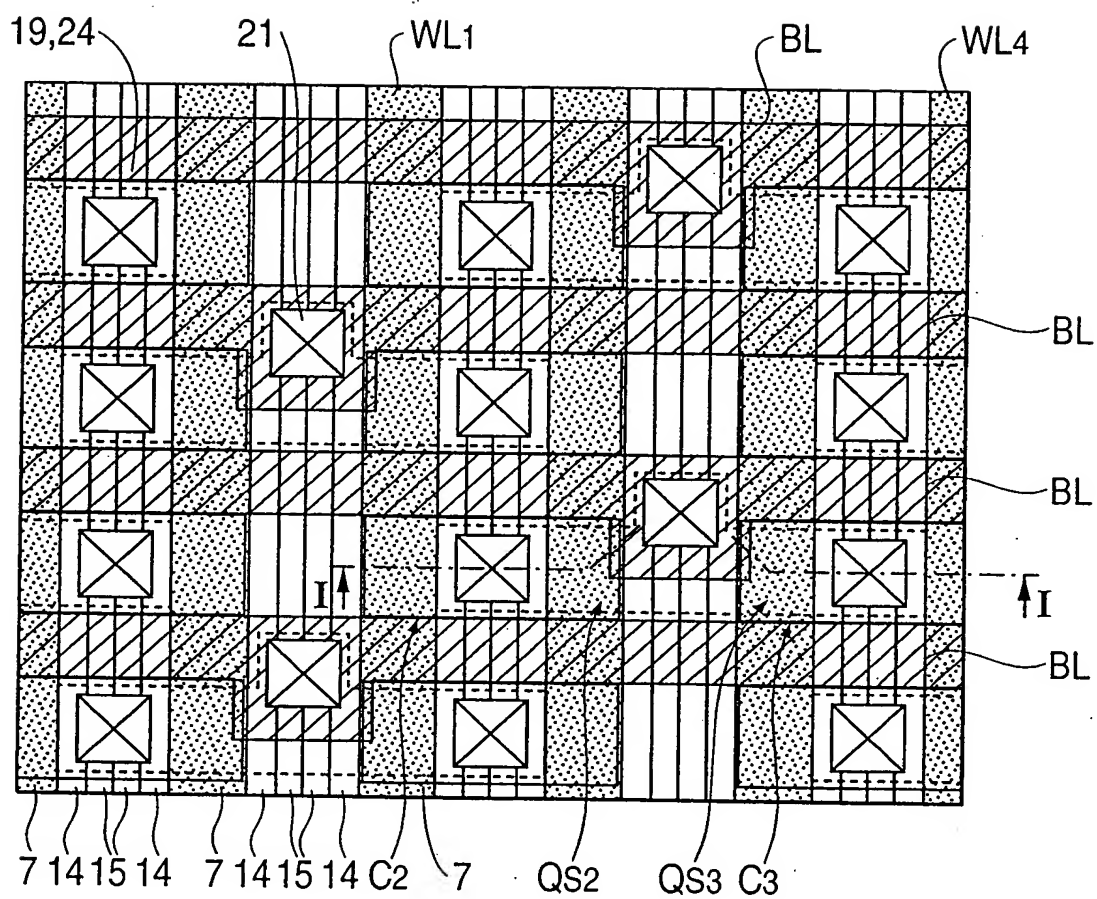


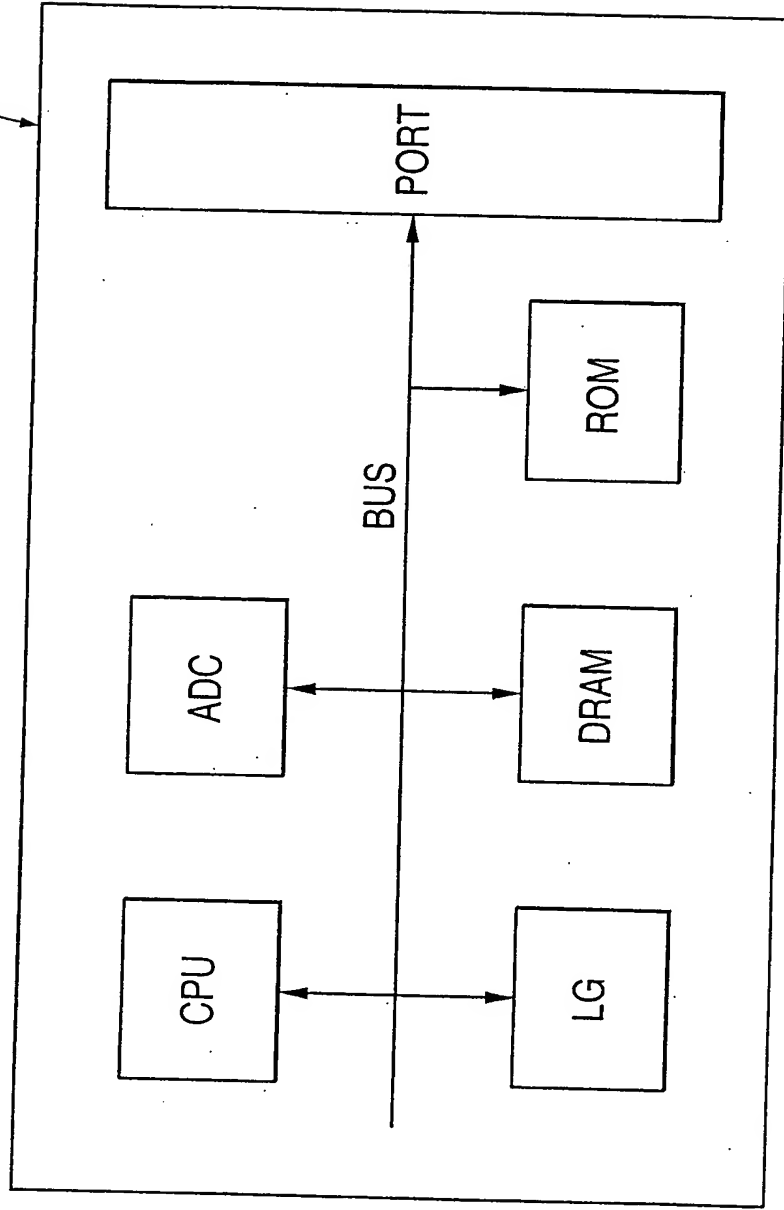
FIG. 1



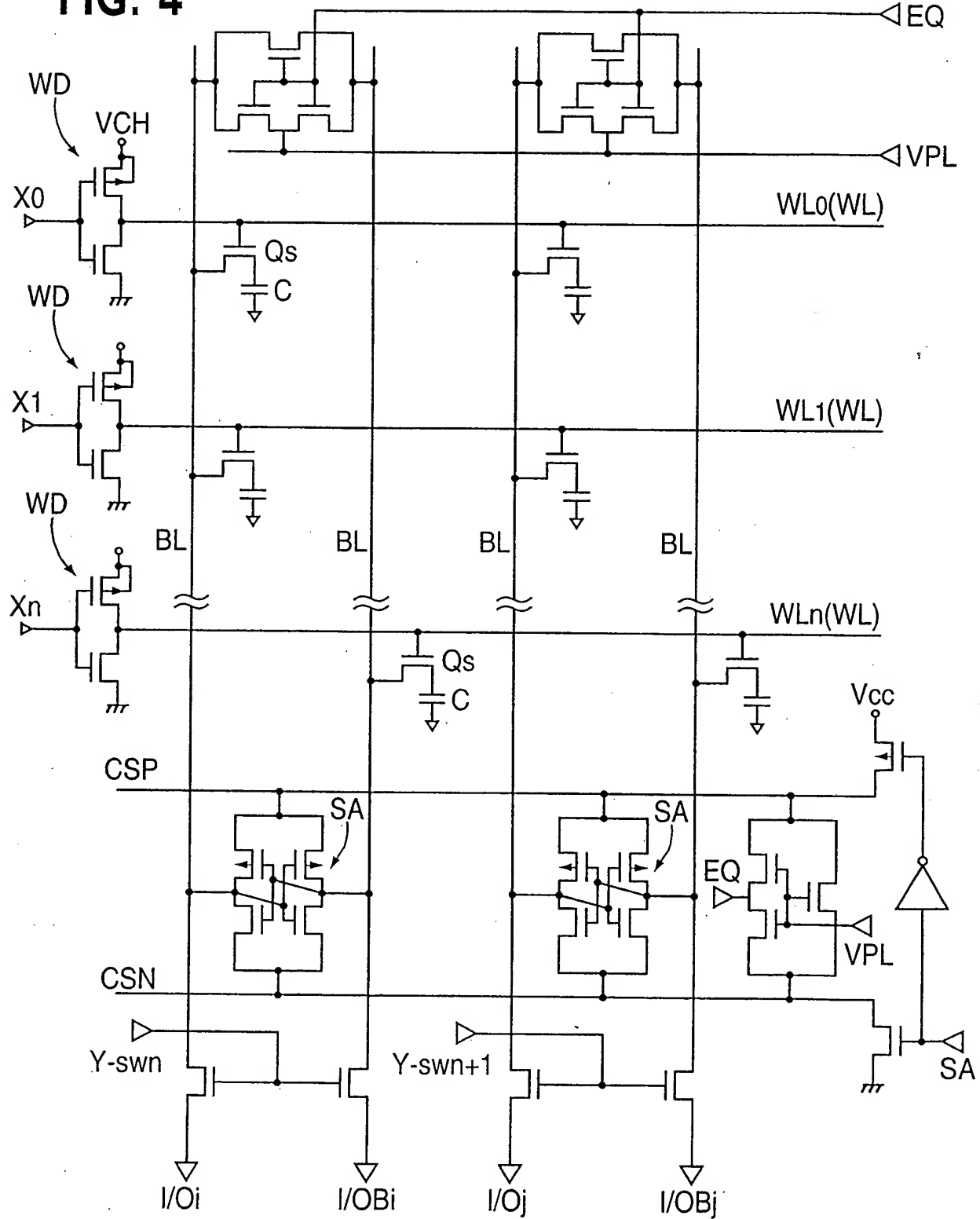
**FIG. 2**



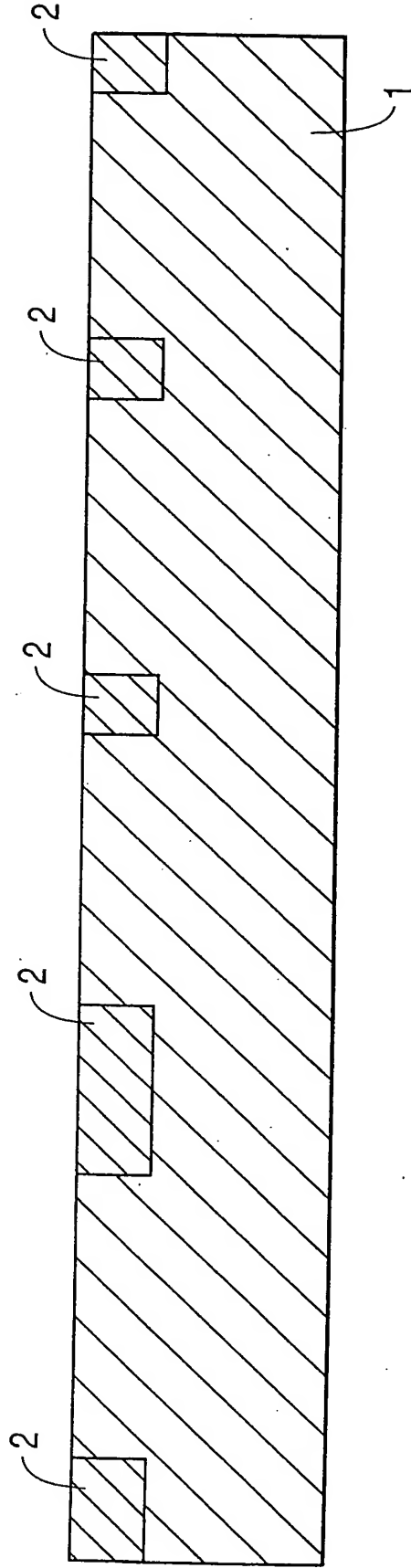
**FIG. 3**



**FIG. 4**



**FIG. 5**



**FIG. 6**

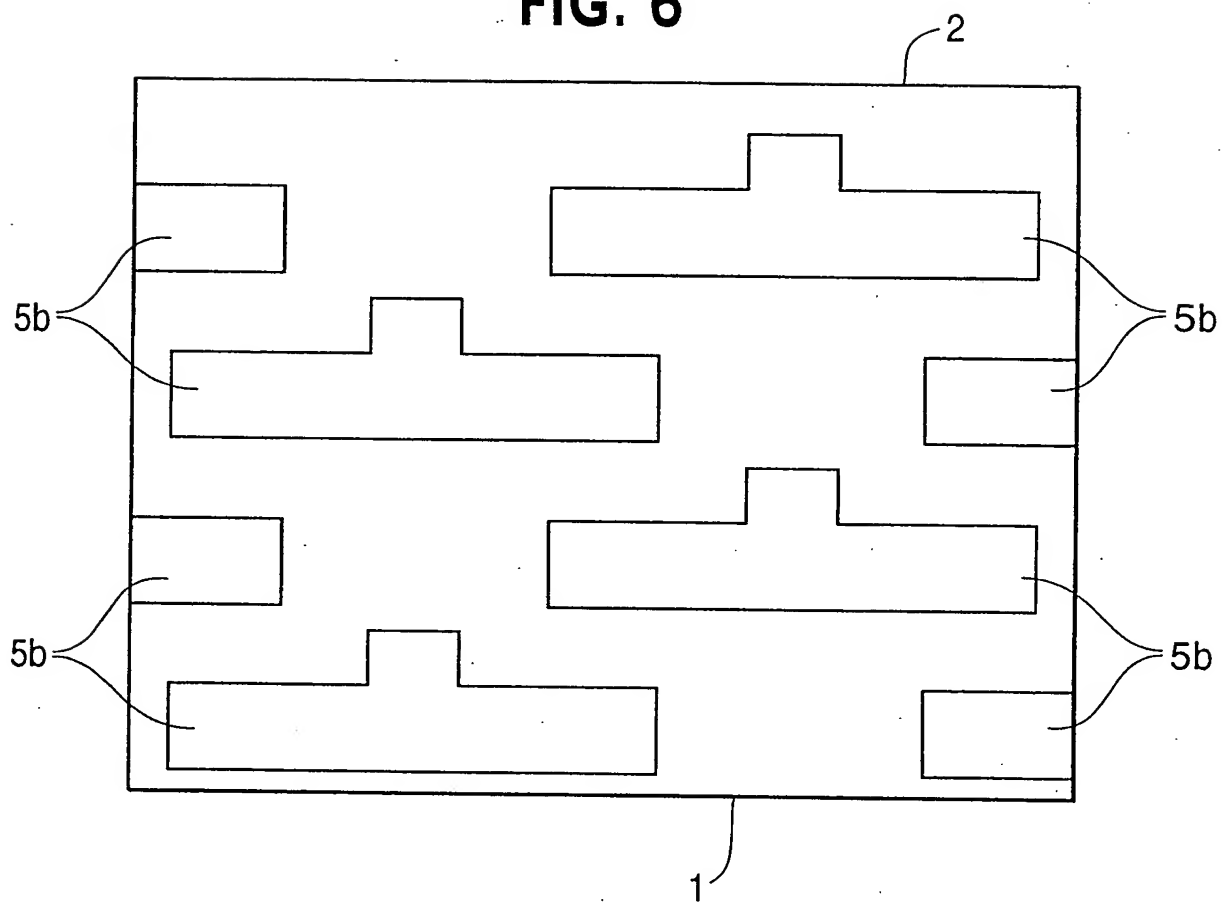
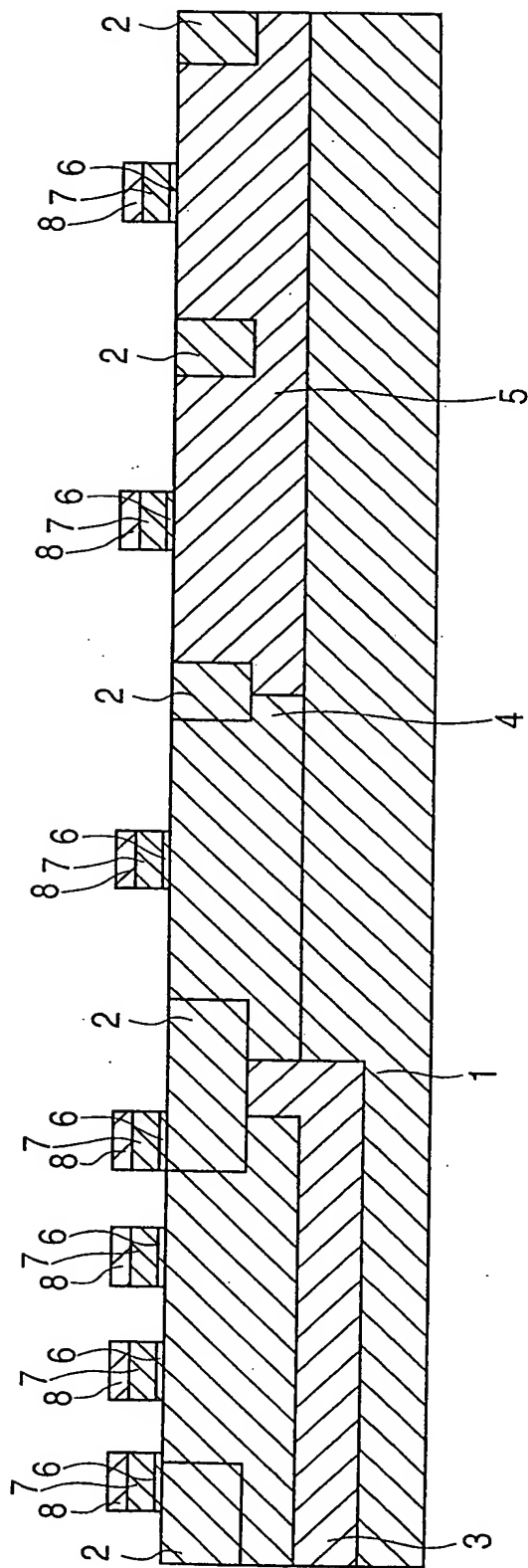




FIG. 8





**FIG. 9**

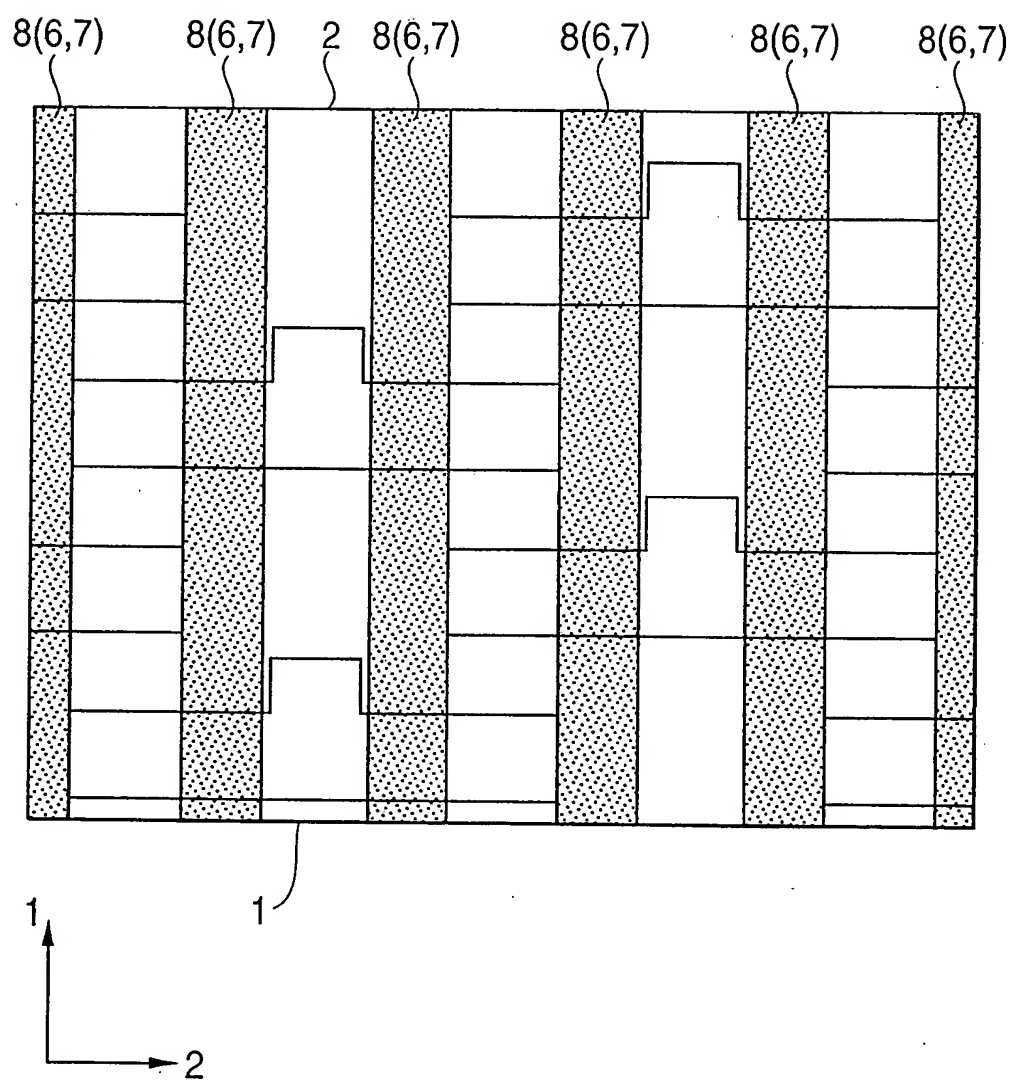
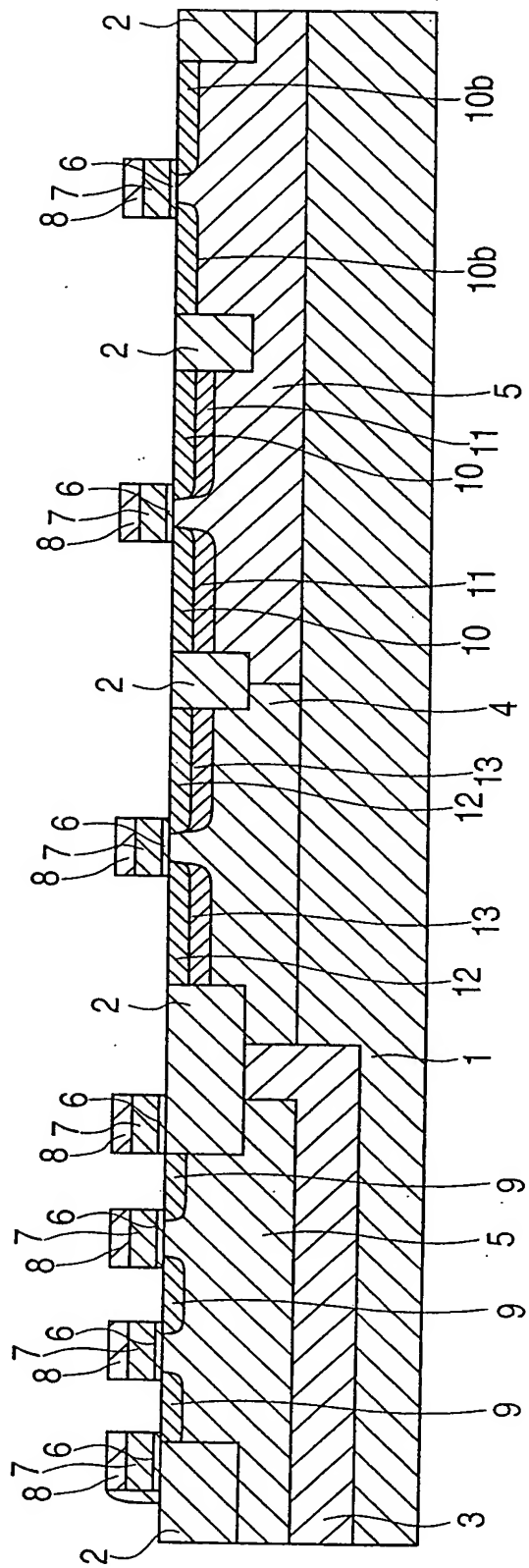


FIG. 10



**FIG. 11**

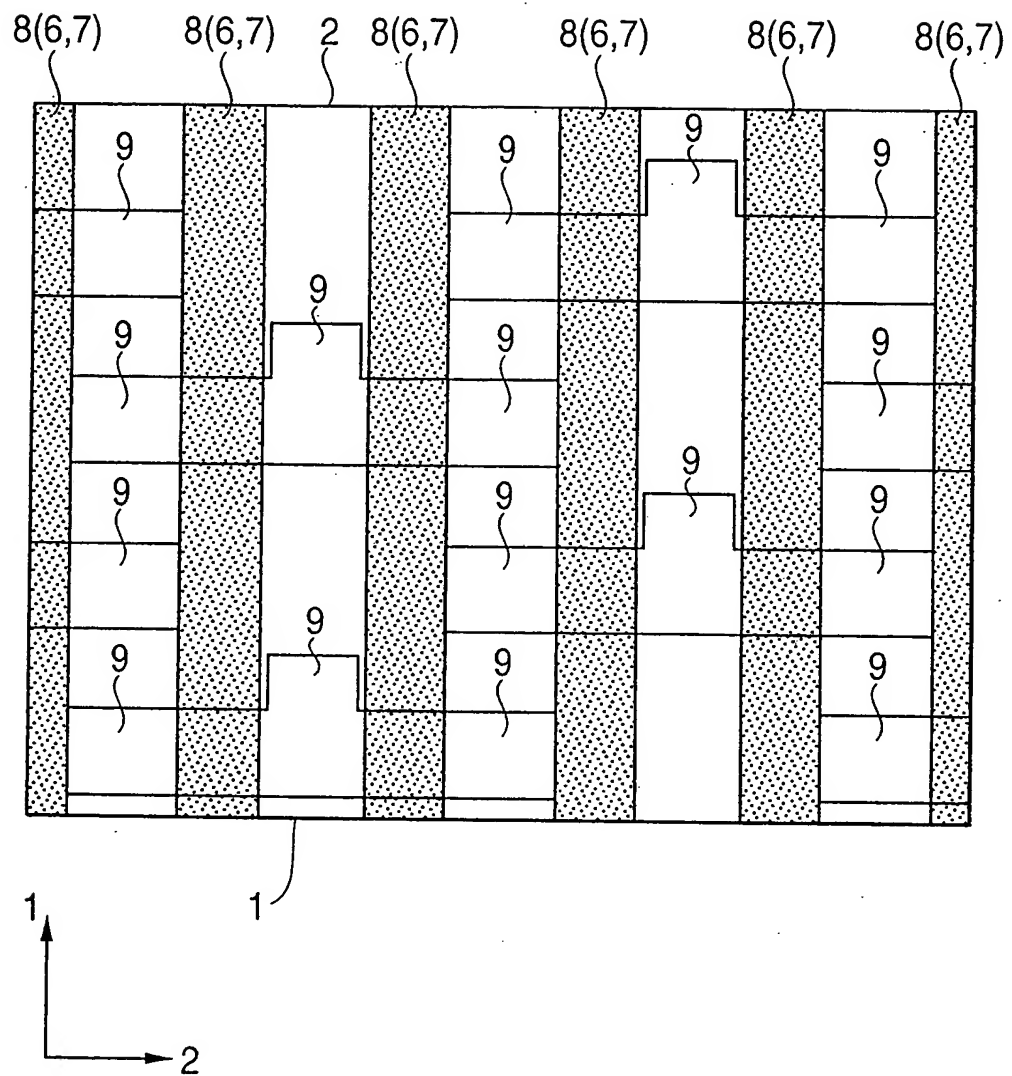
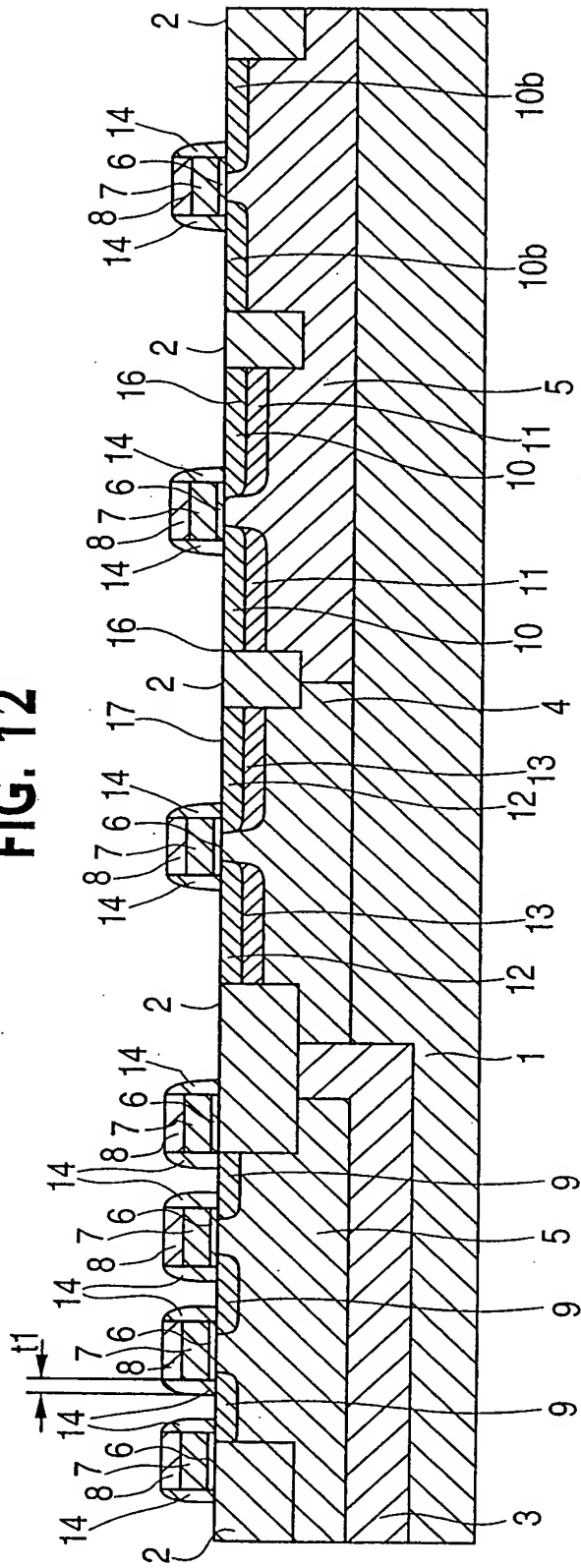
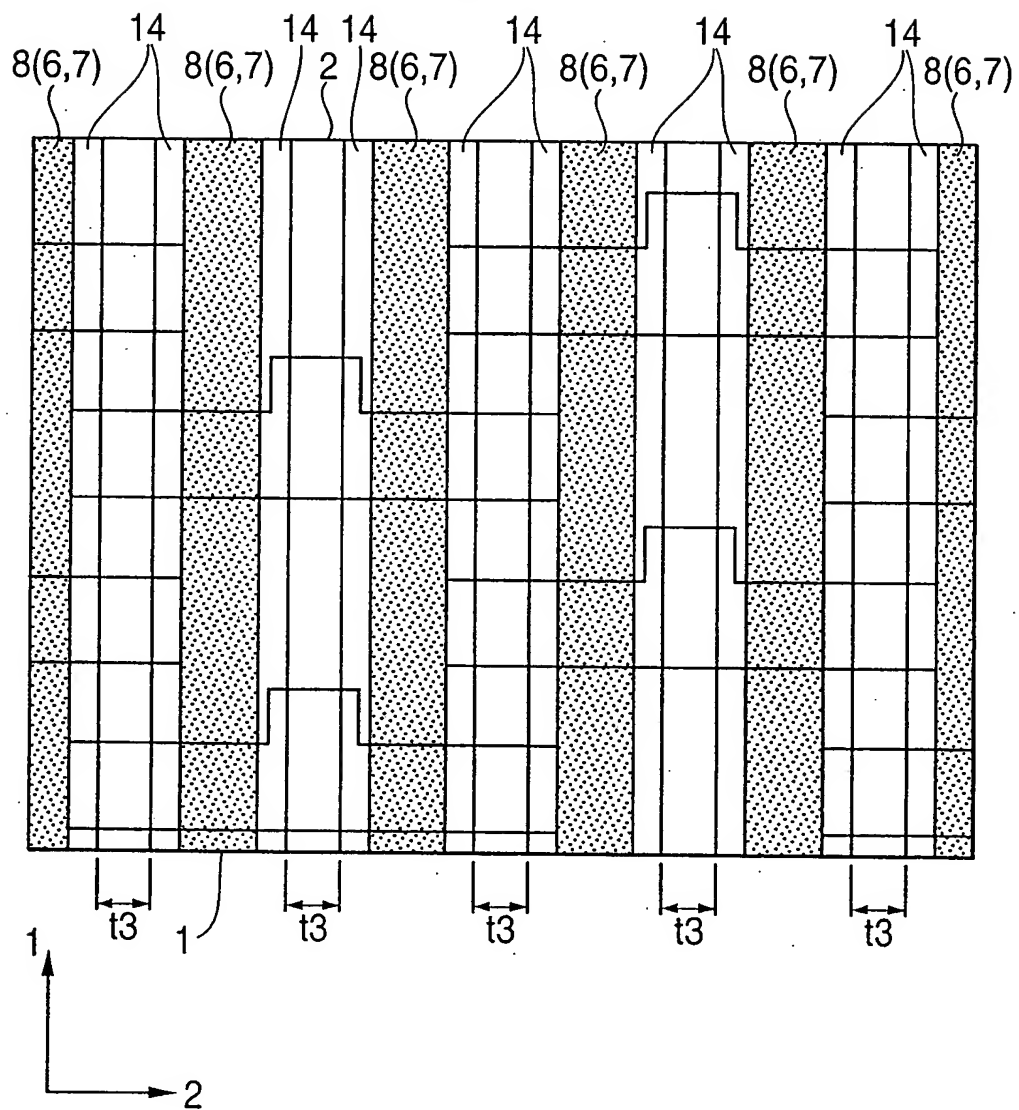
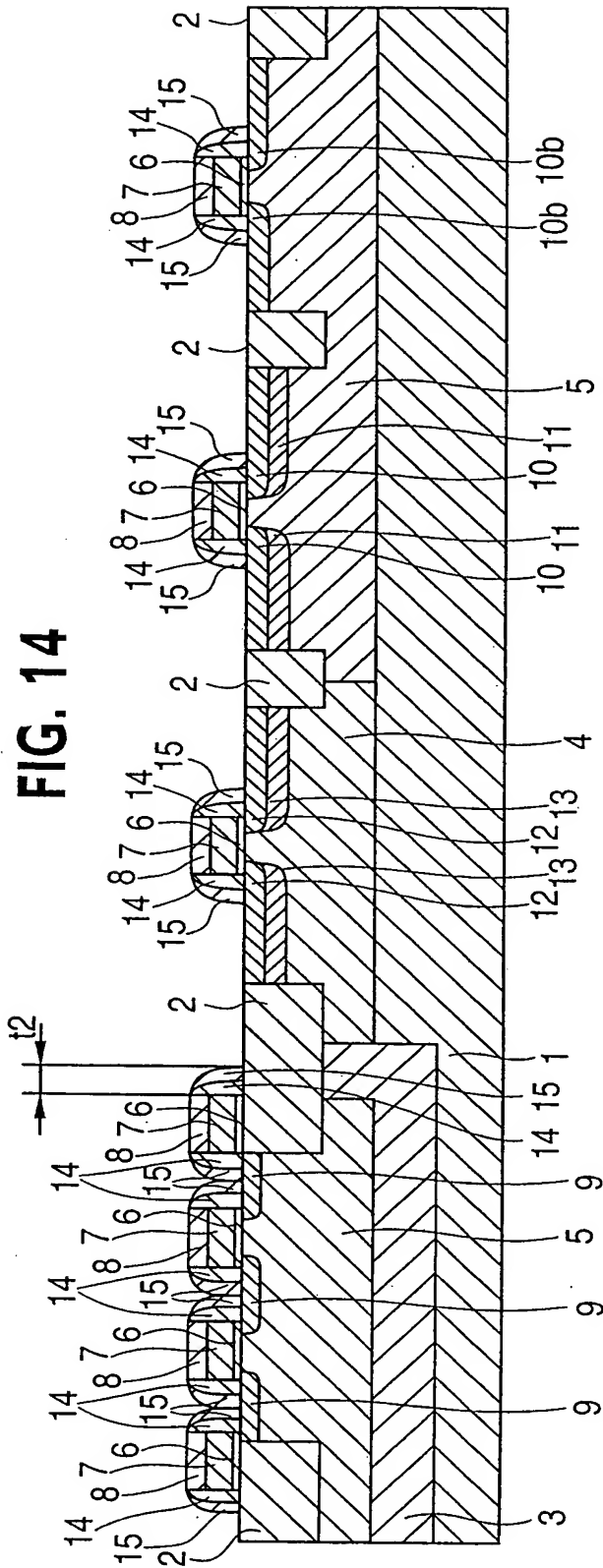


FIG. 12



**FIG. 13**





**FIG. 14**

**FIG. 15**

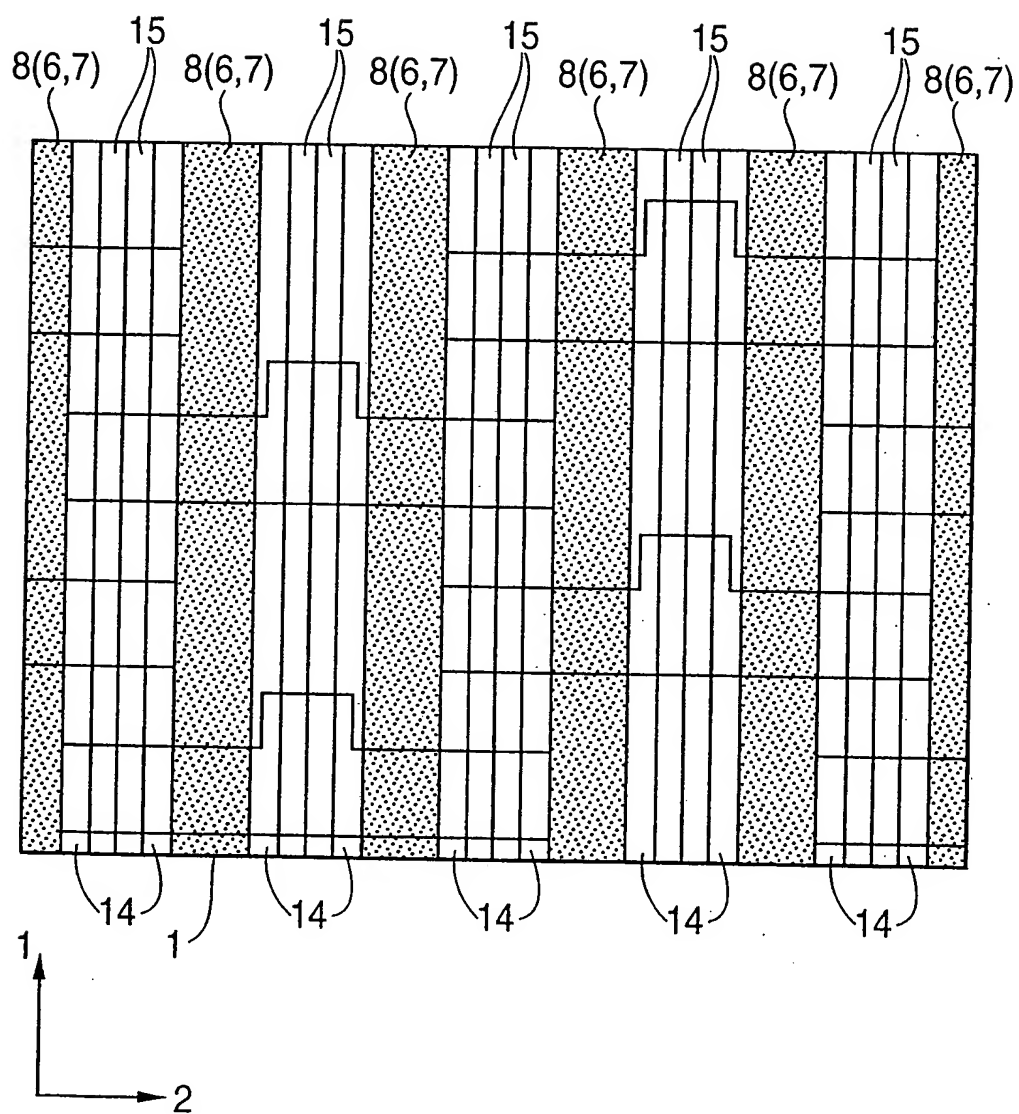


FIG. 16

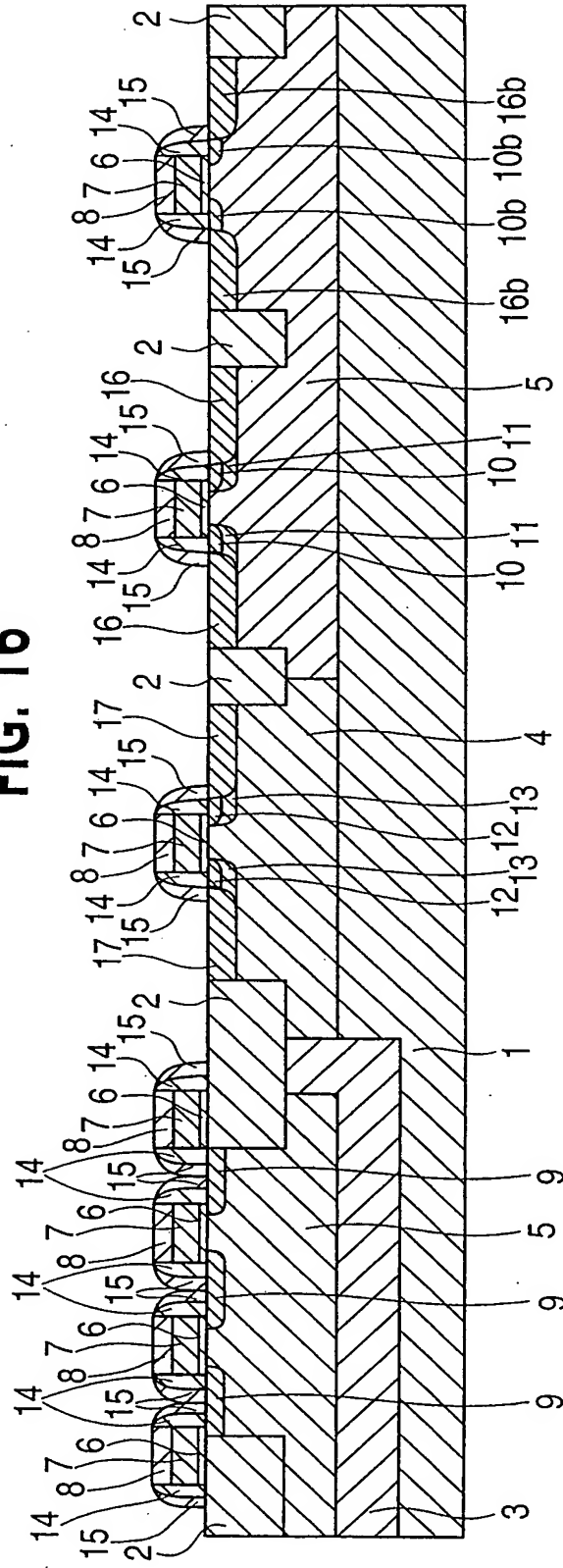
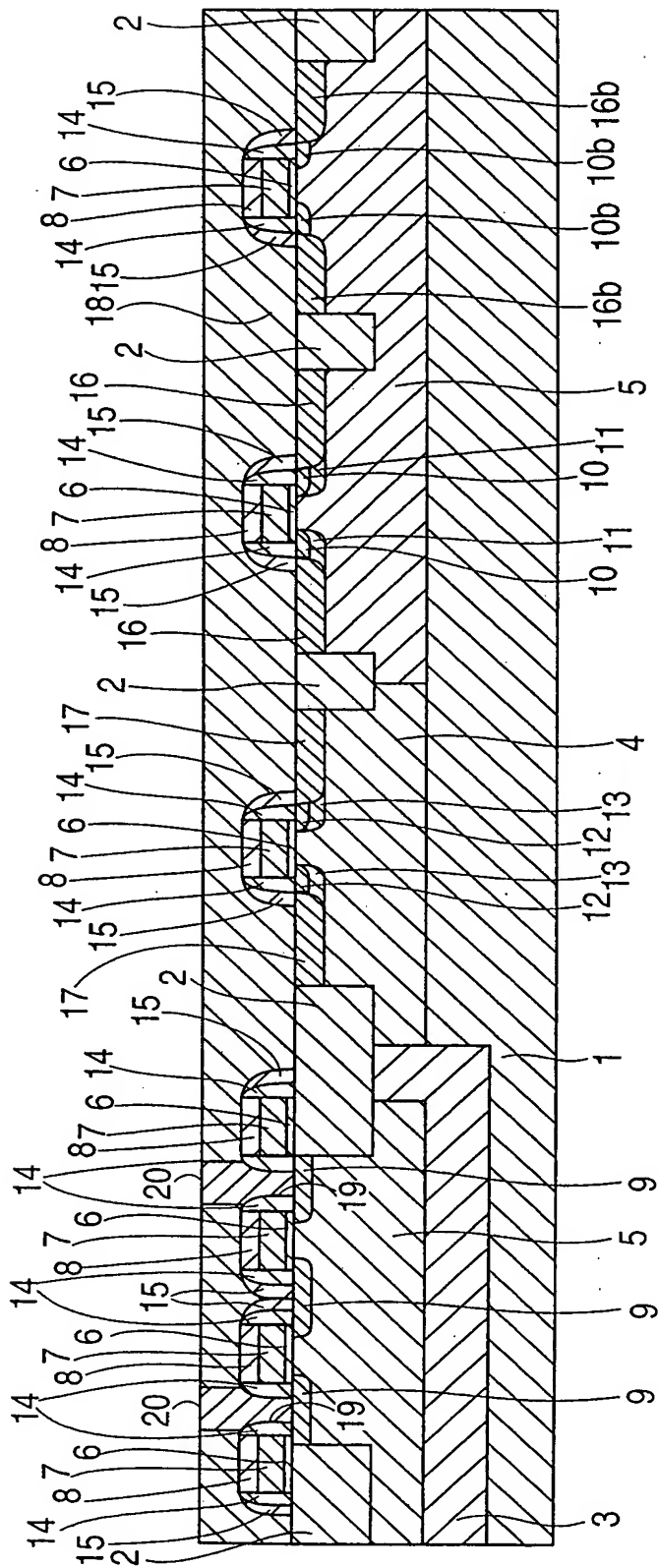




FIG. 17



**FIG. 18**

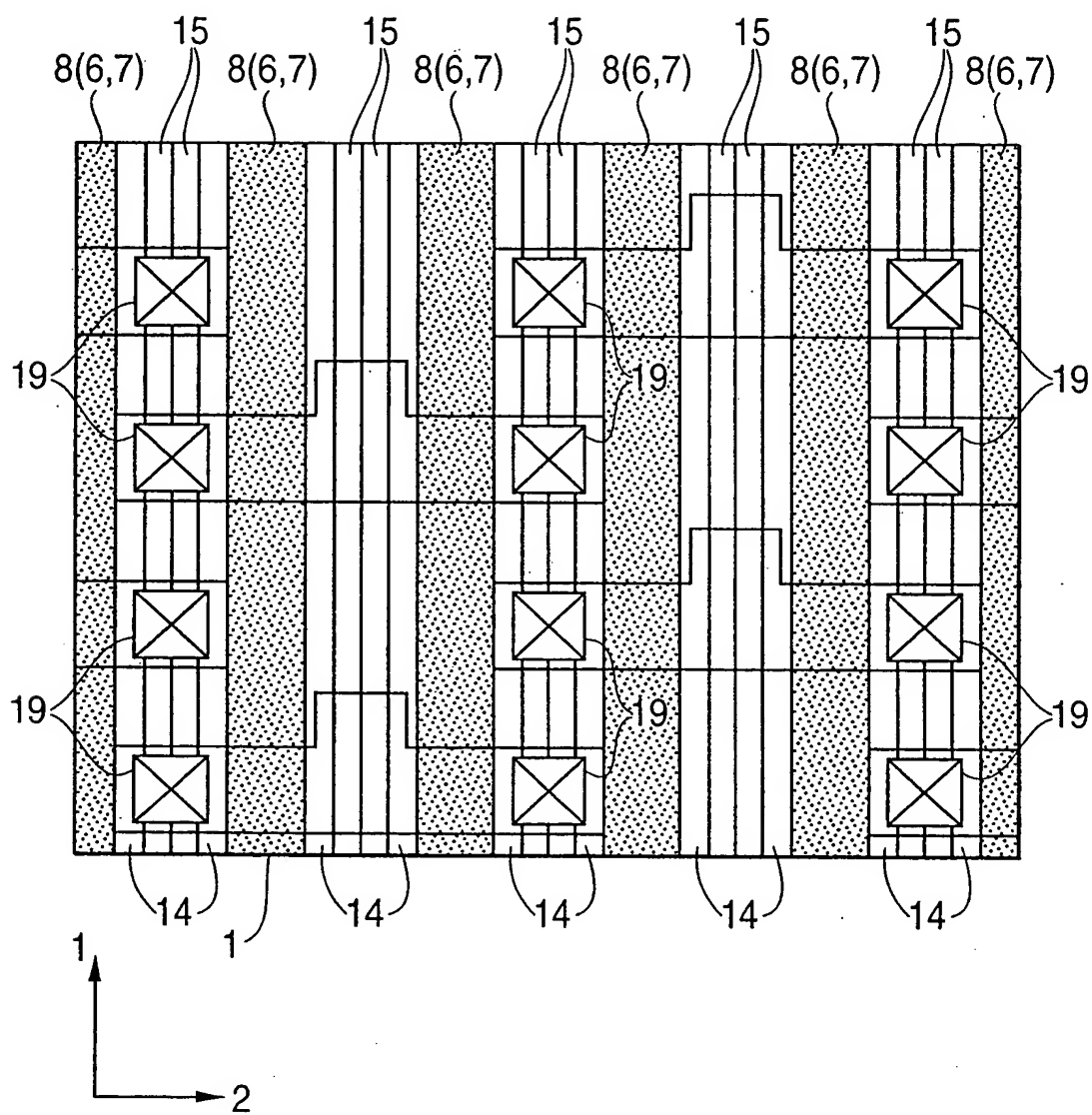
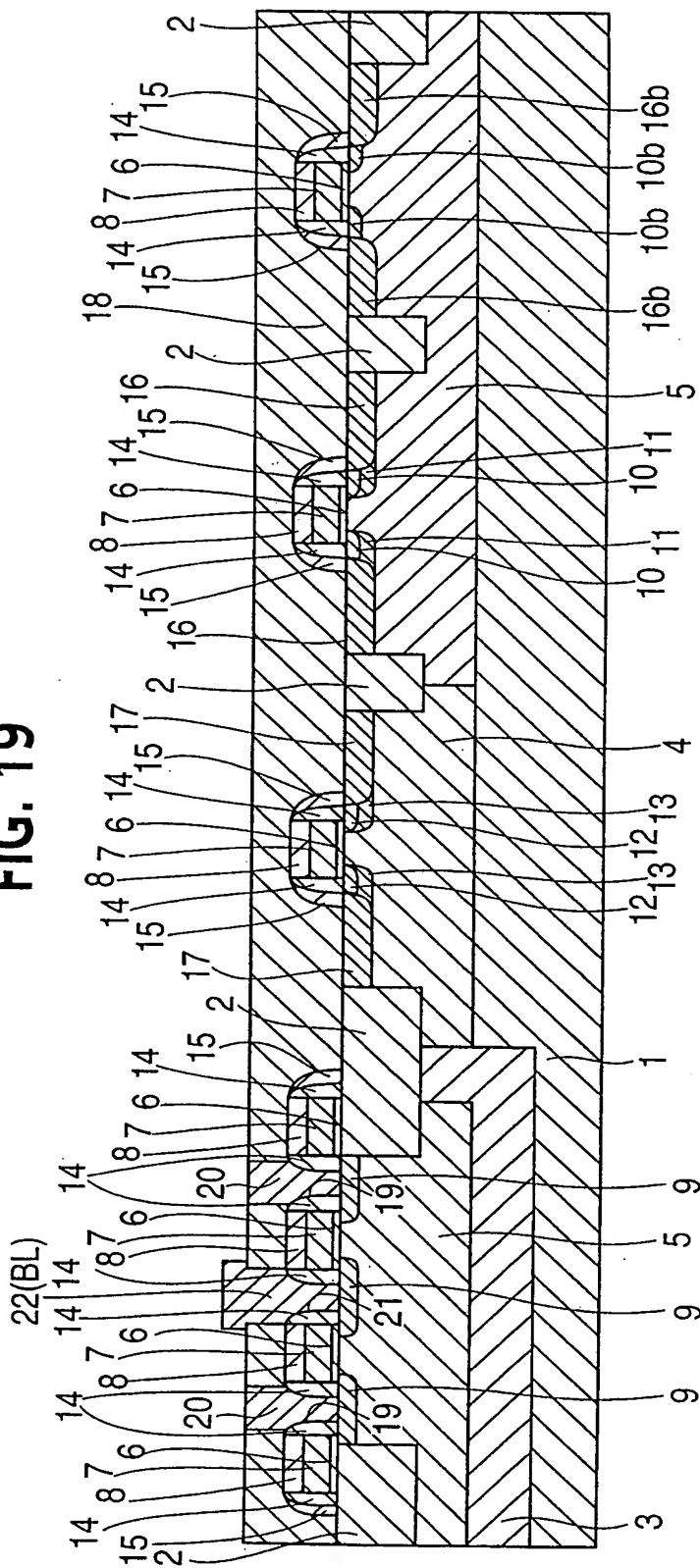
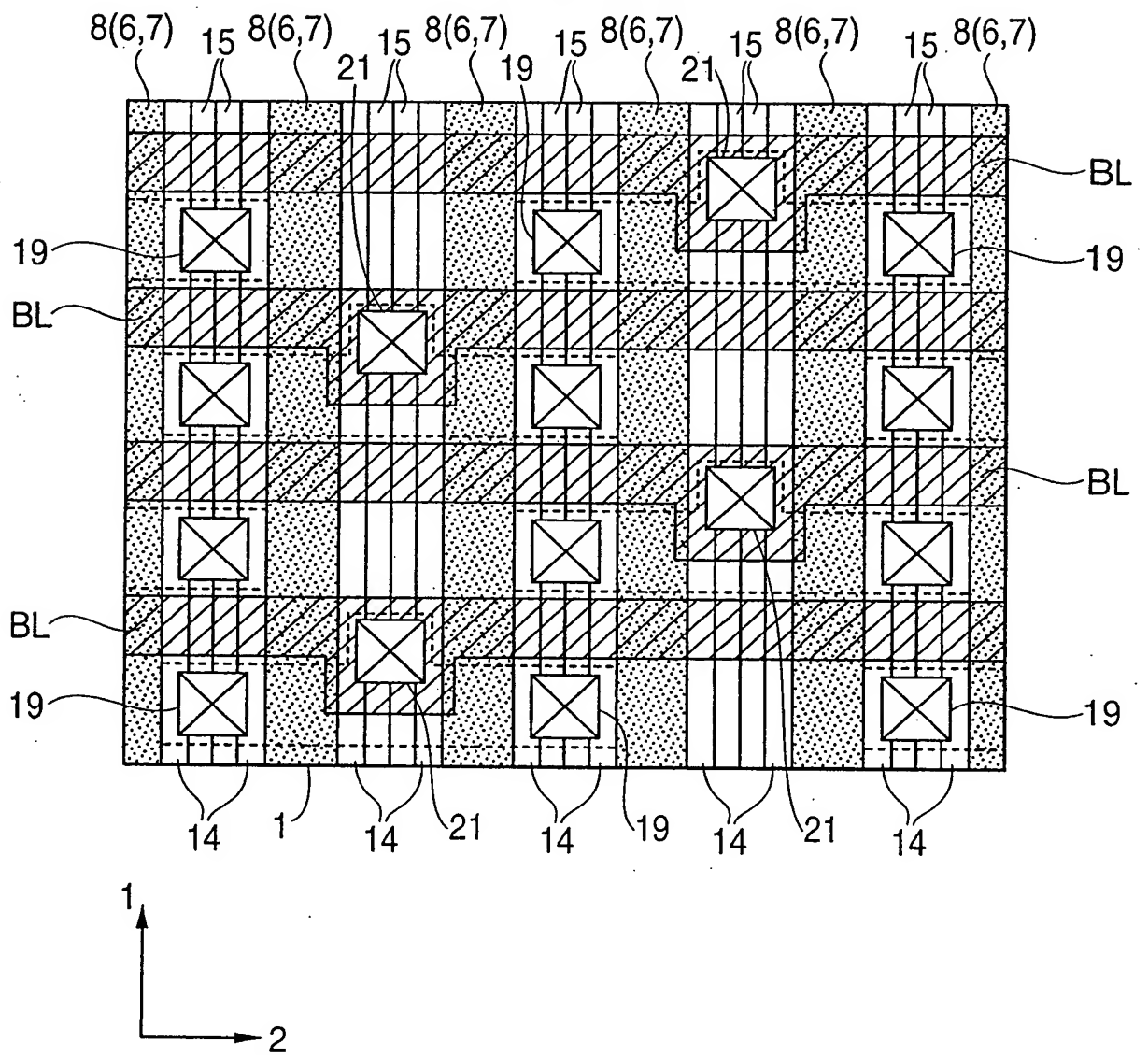
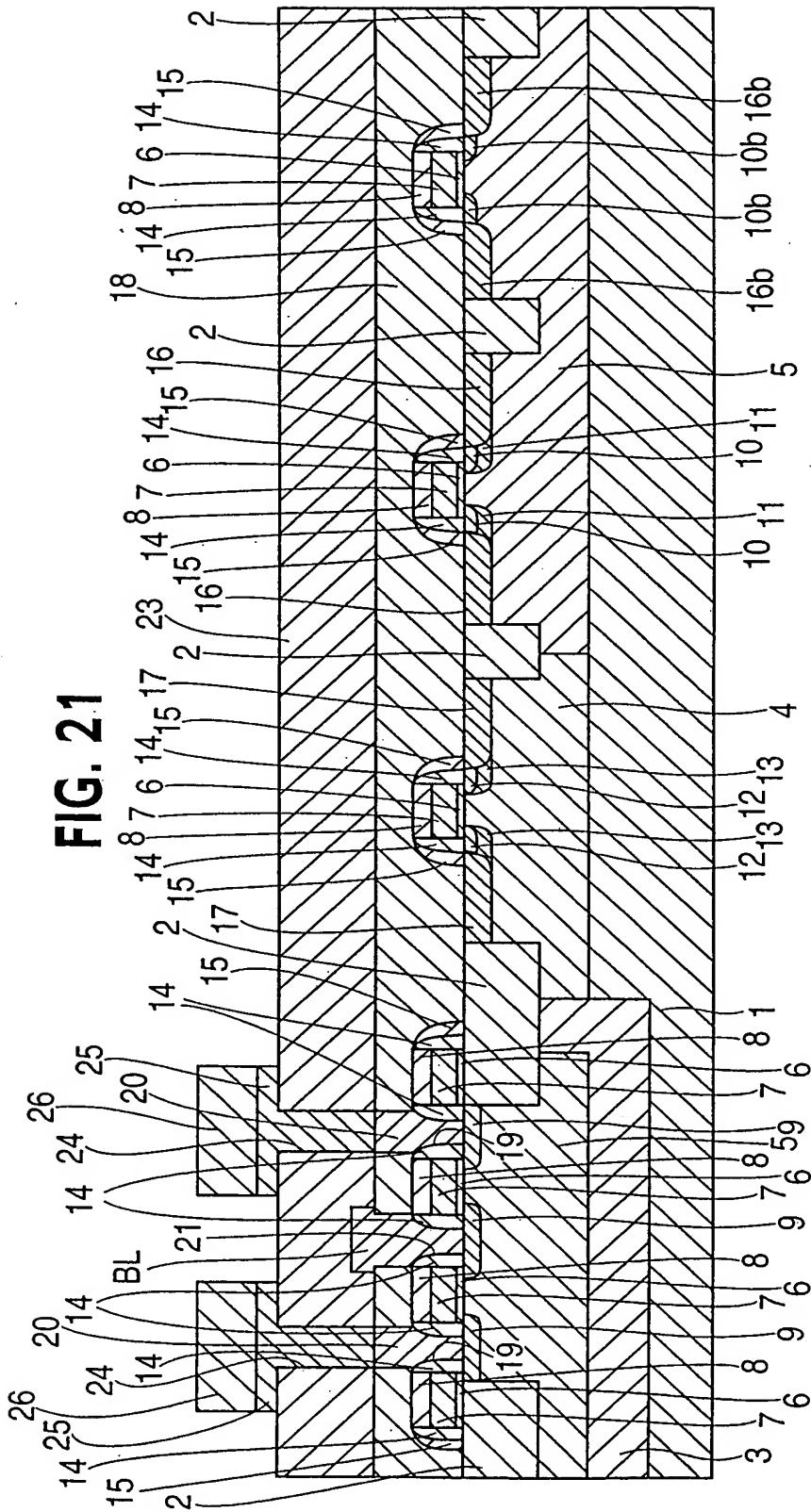


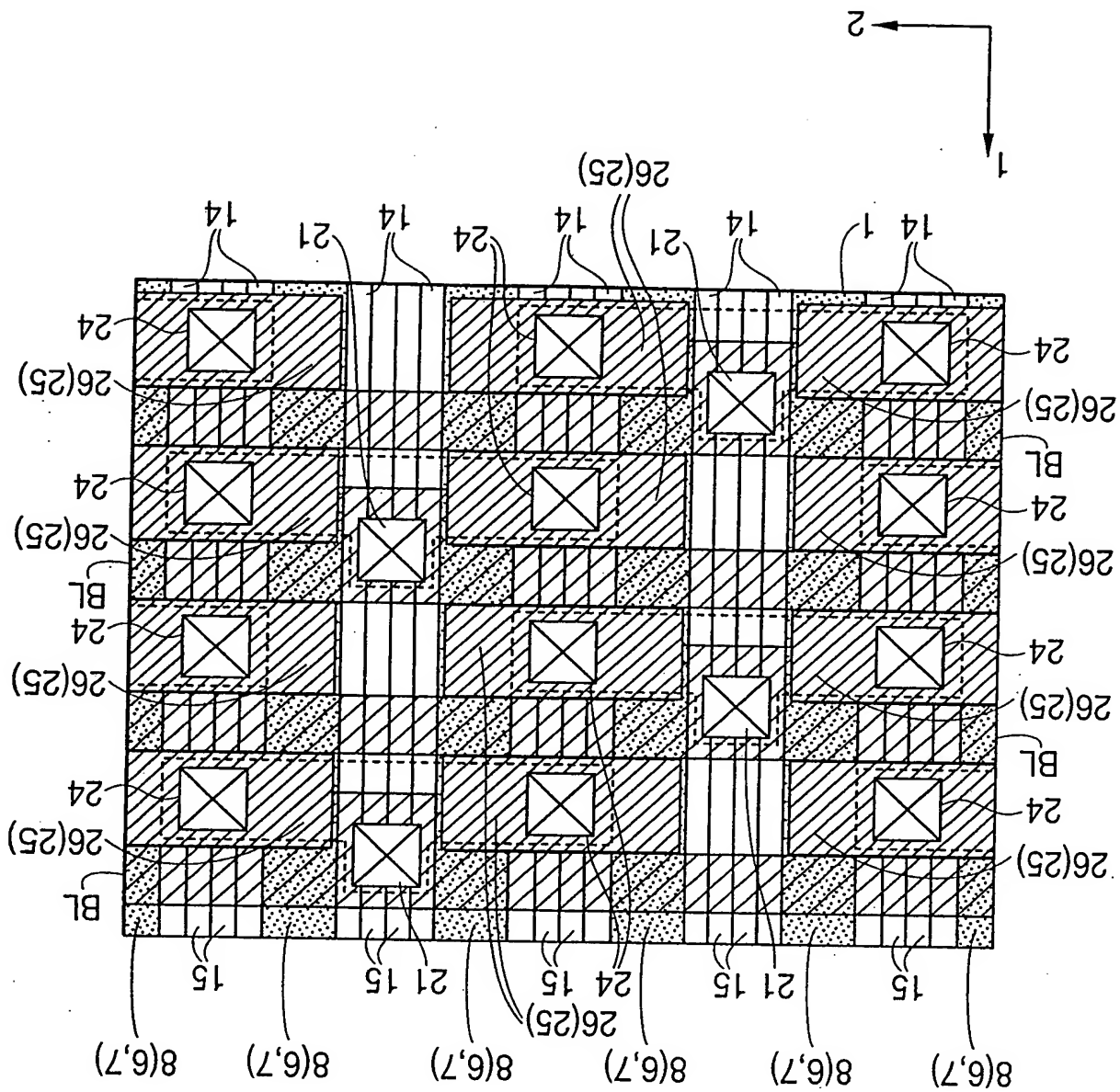
FIG. 19



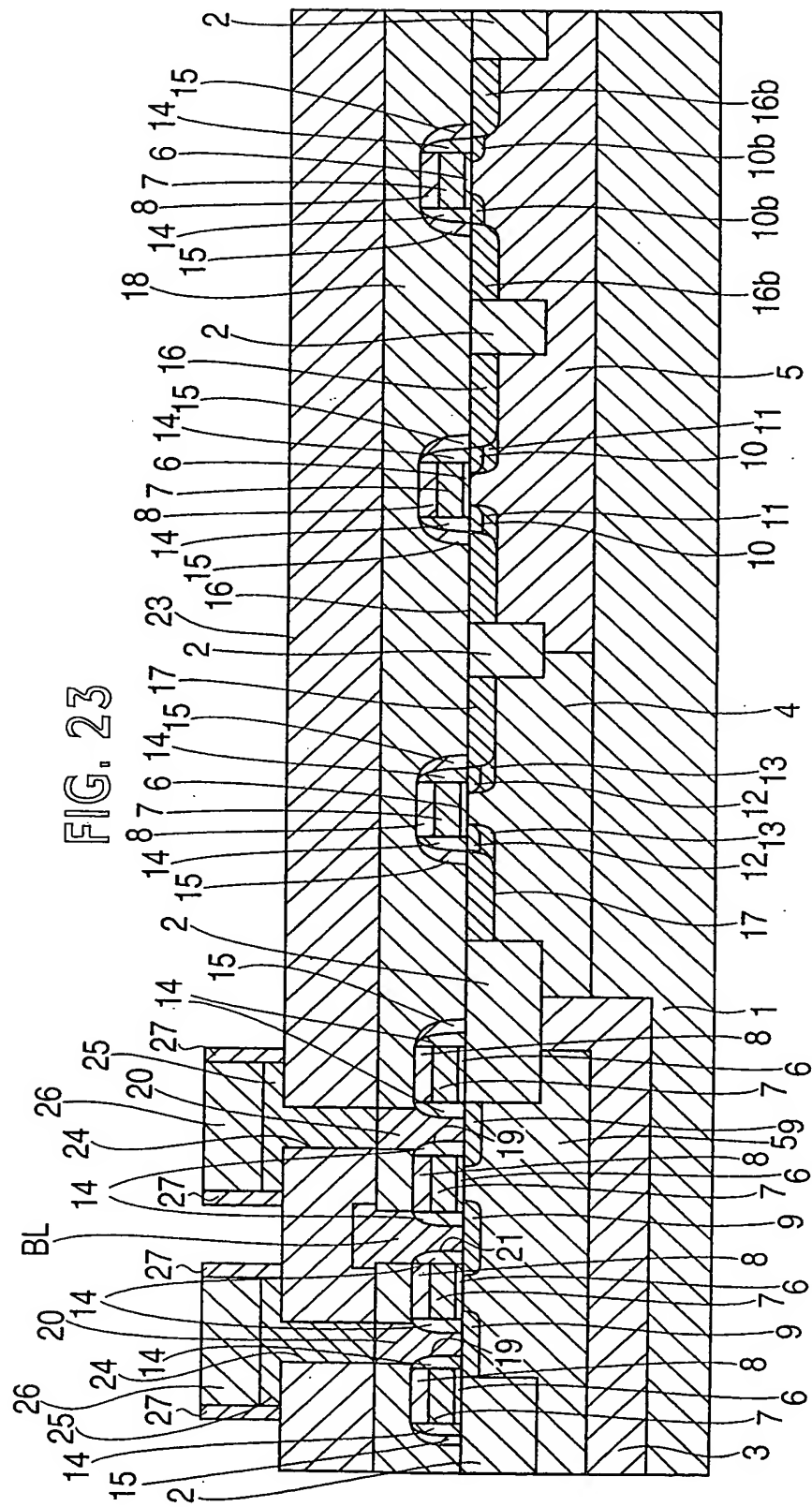
**FIG. 20**

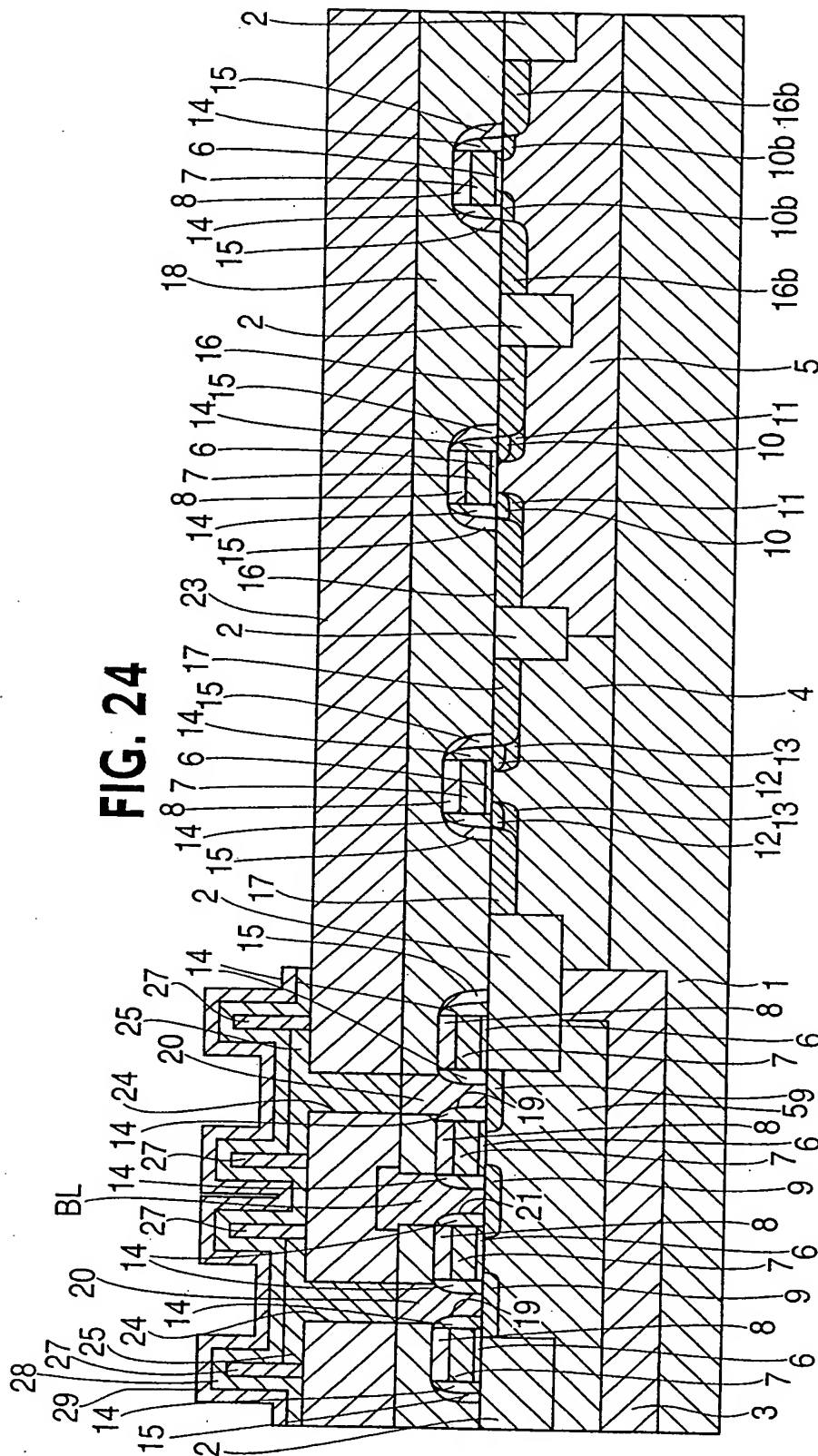






**FIG. 22**







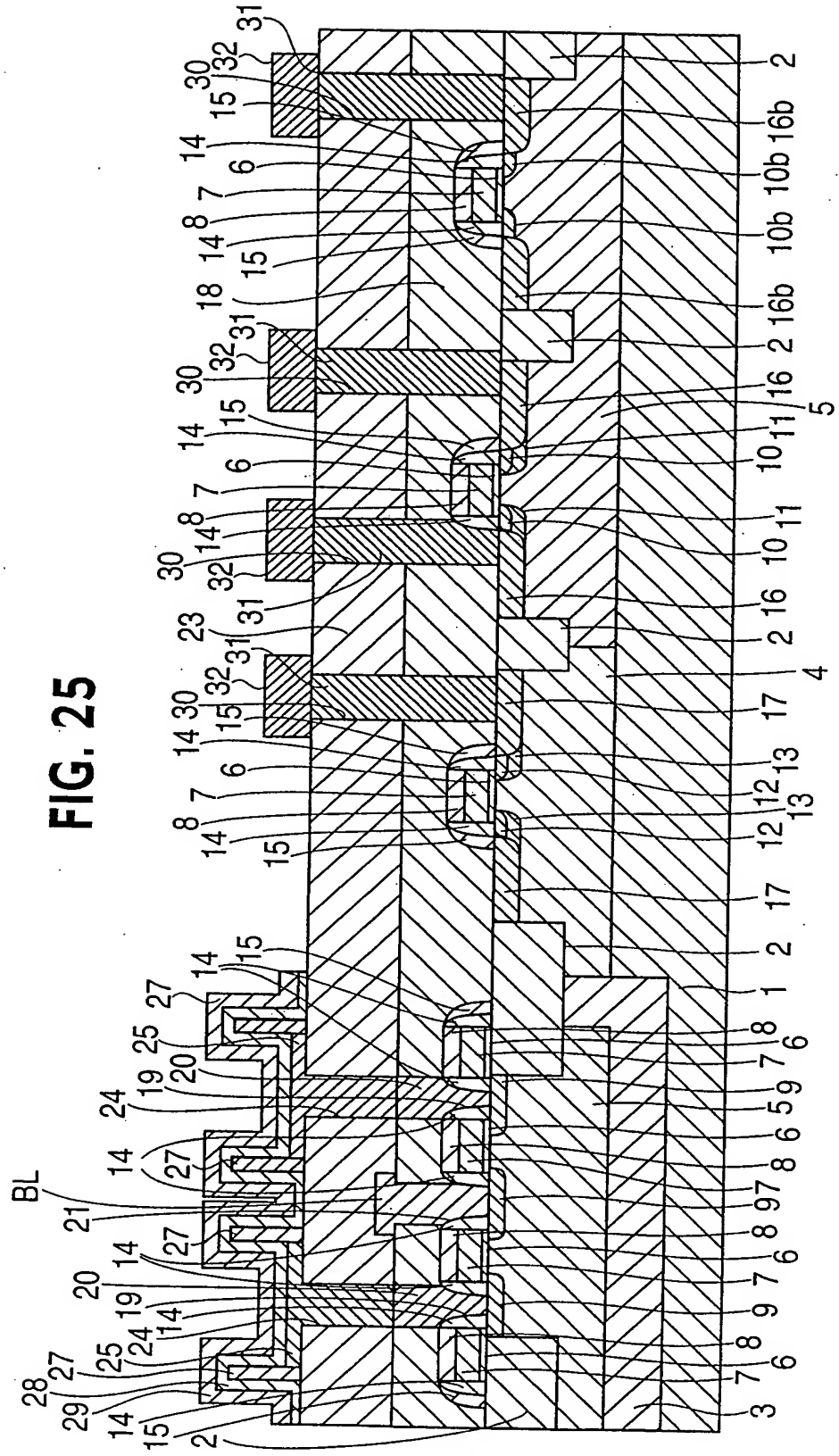


FIG. 25

FIG. 26

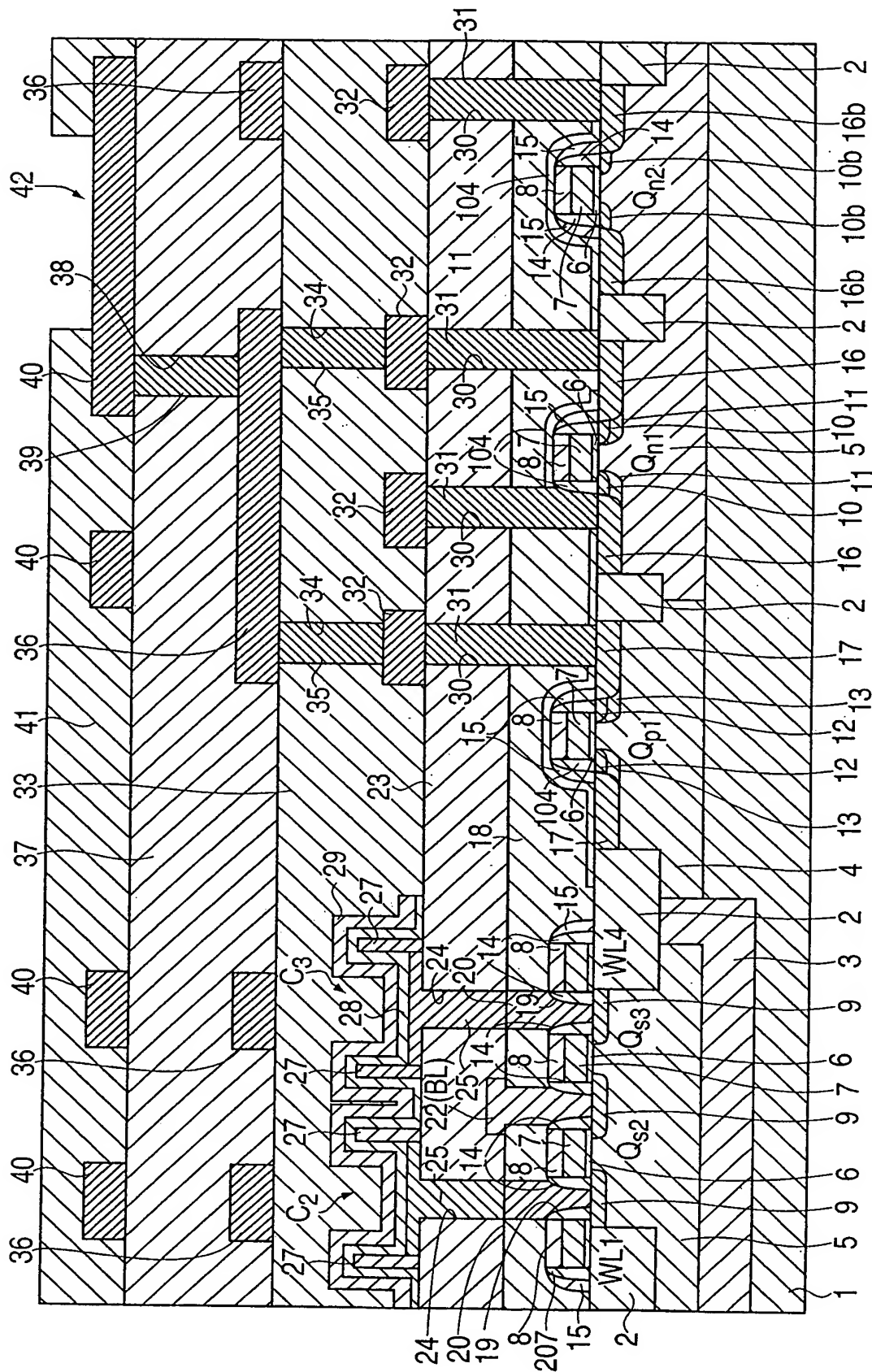


FIG. 27

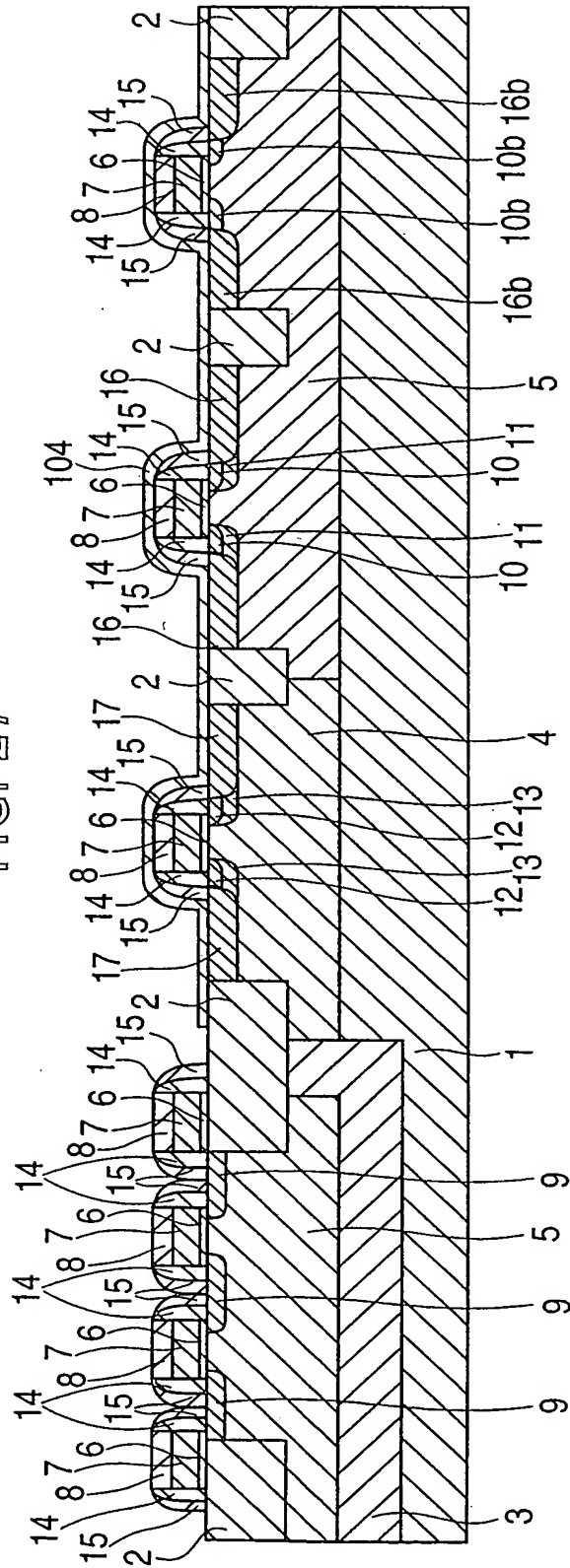


FIG. 28

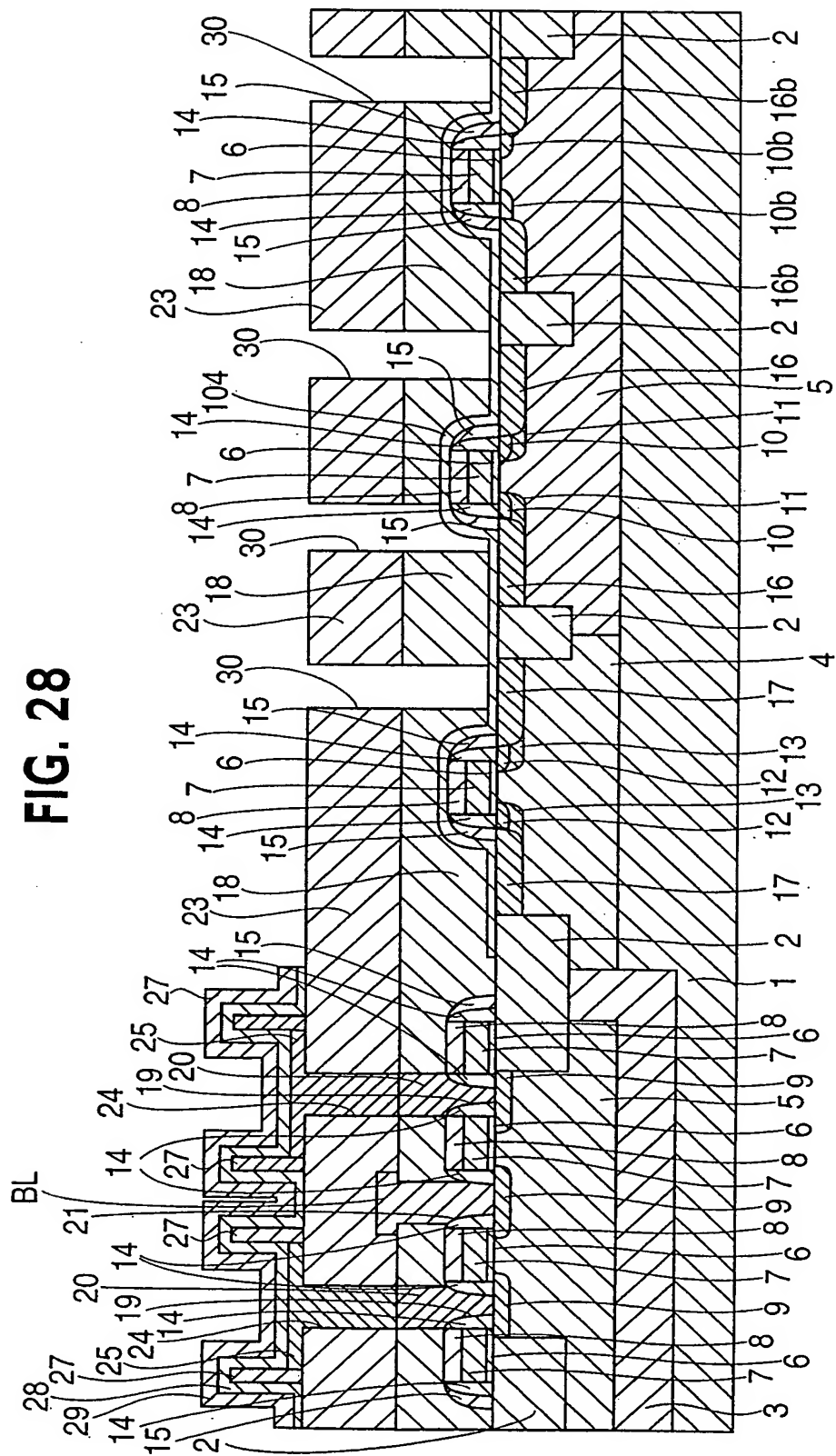
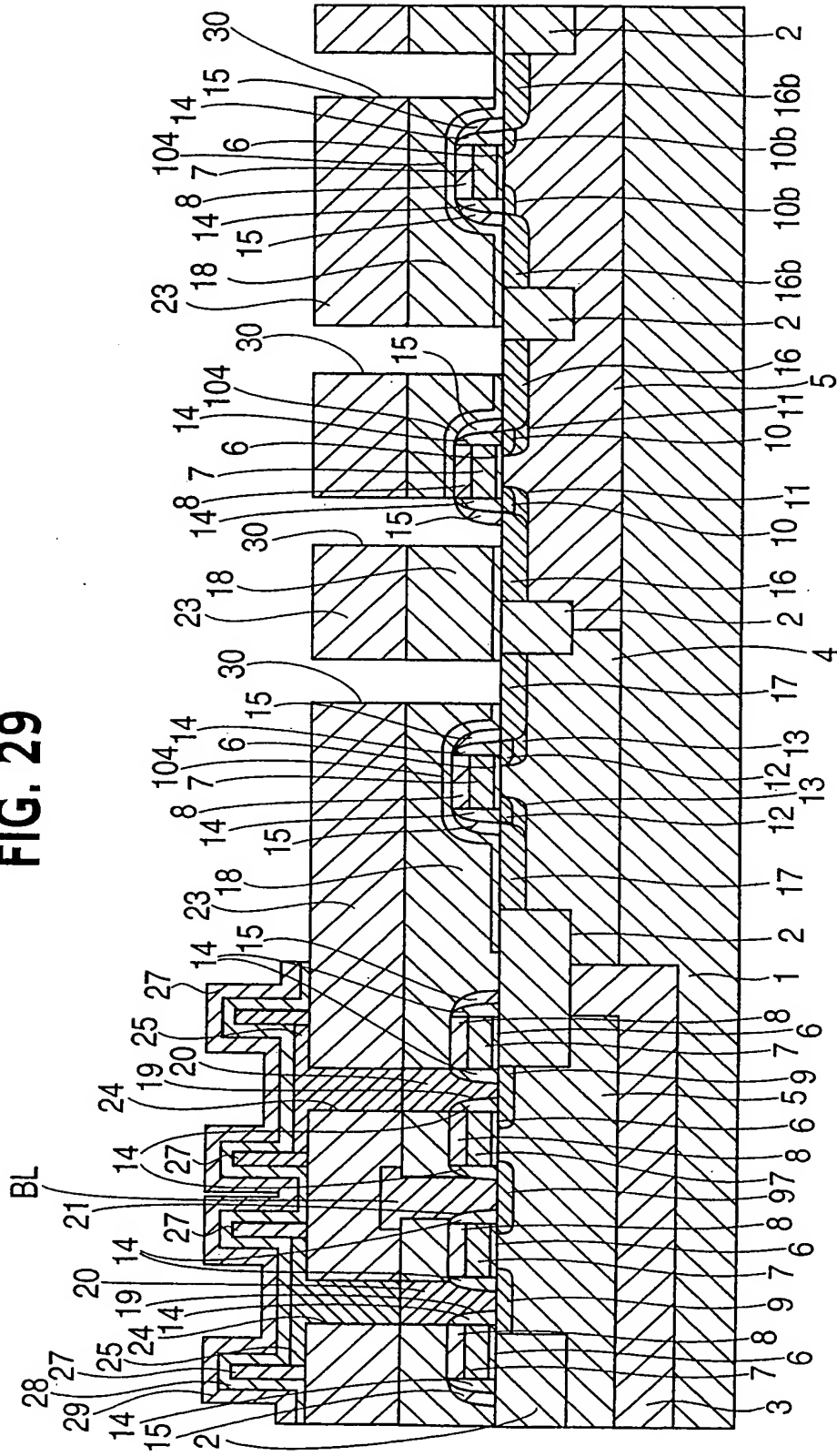


FIG. 29



**FIG. 30**

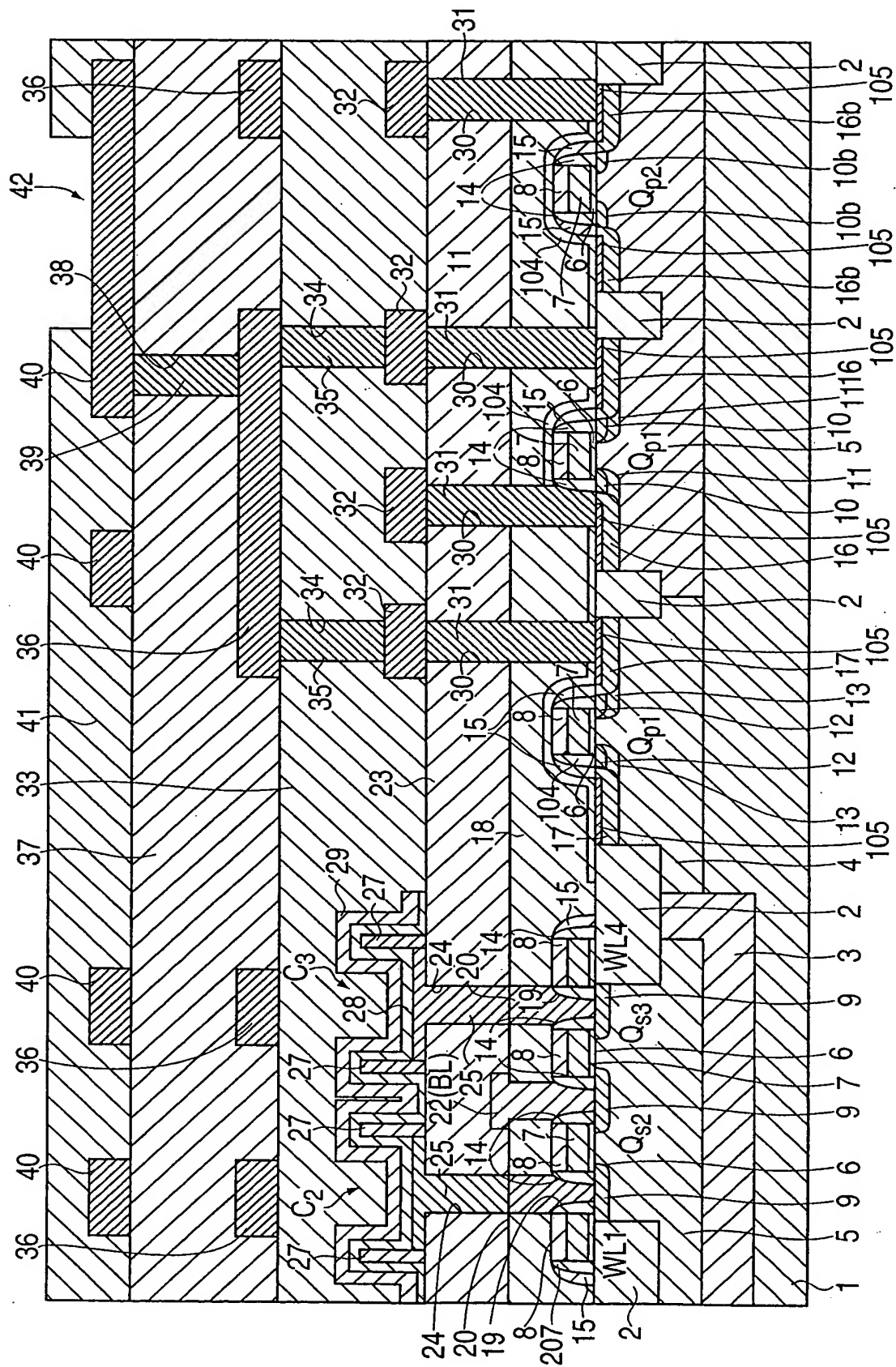


FIG. 31

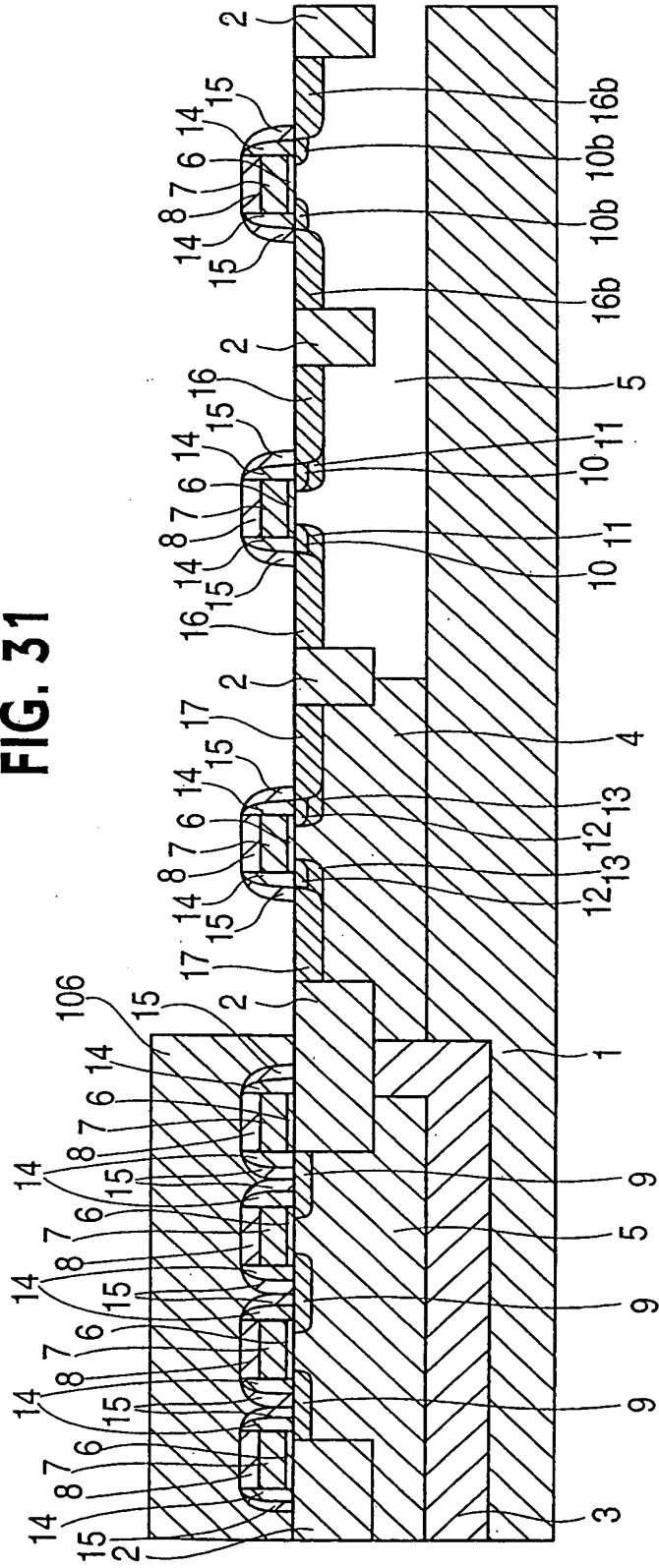


FIG. 32

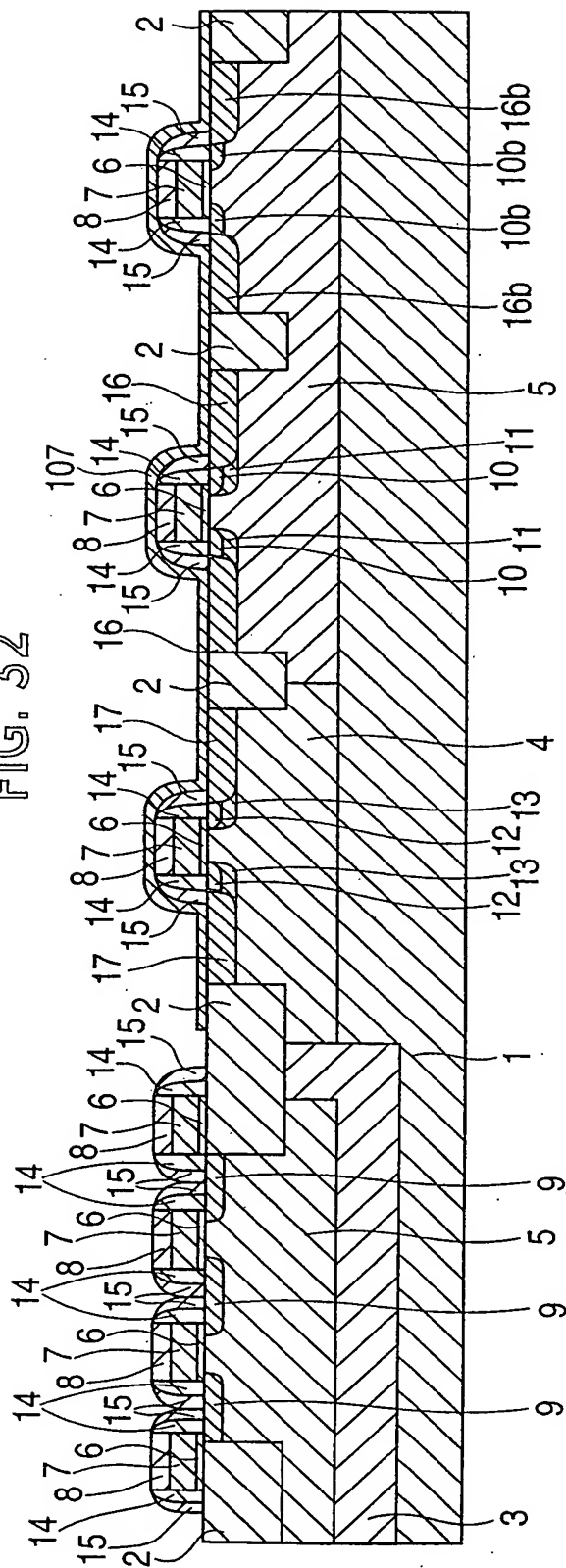




FIG. 33

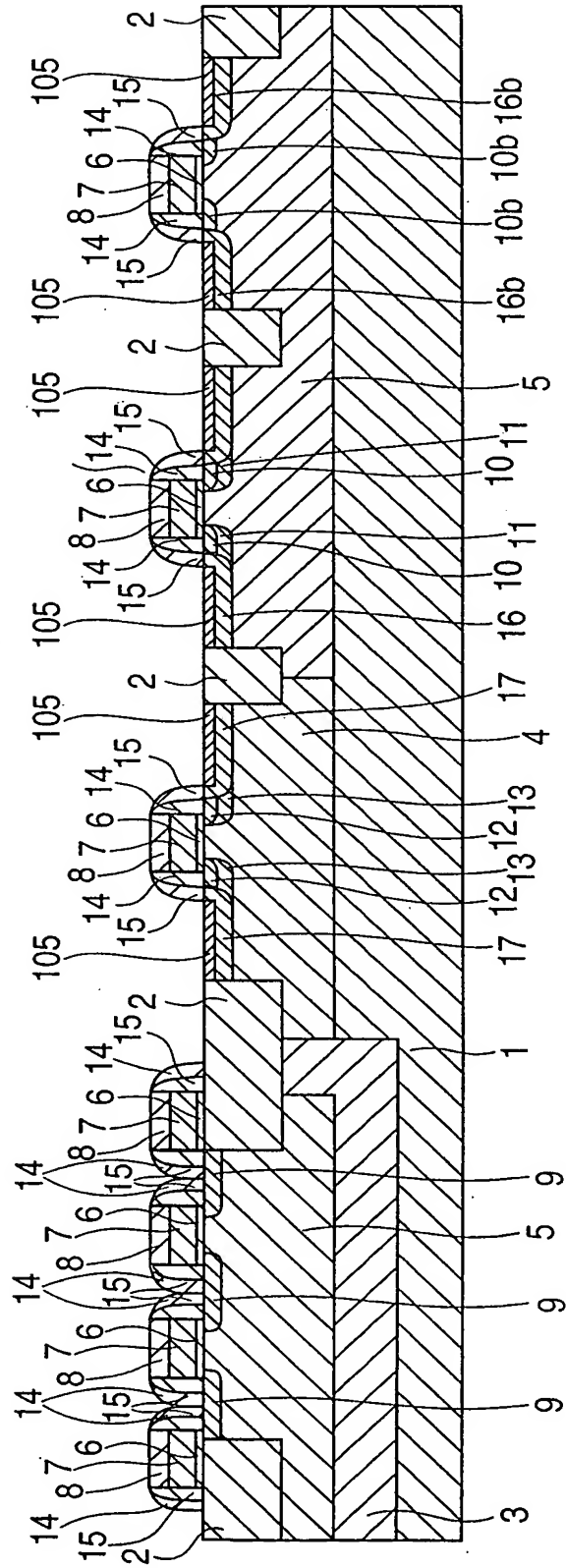
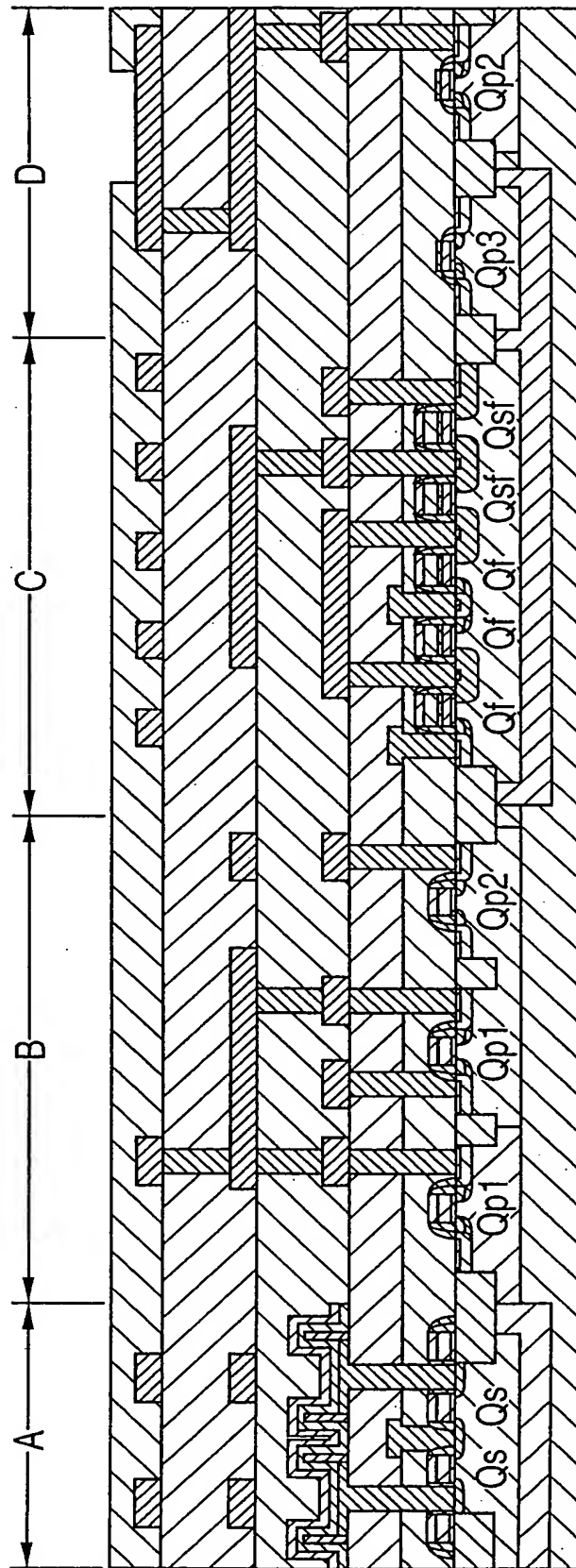
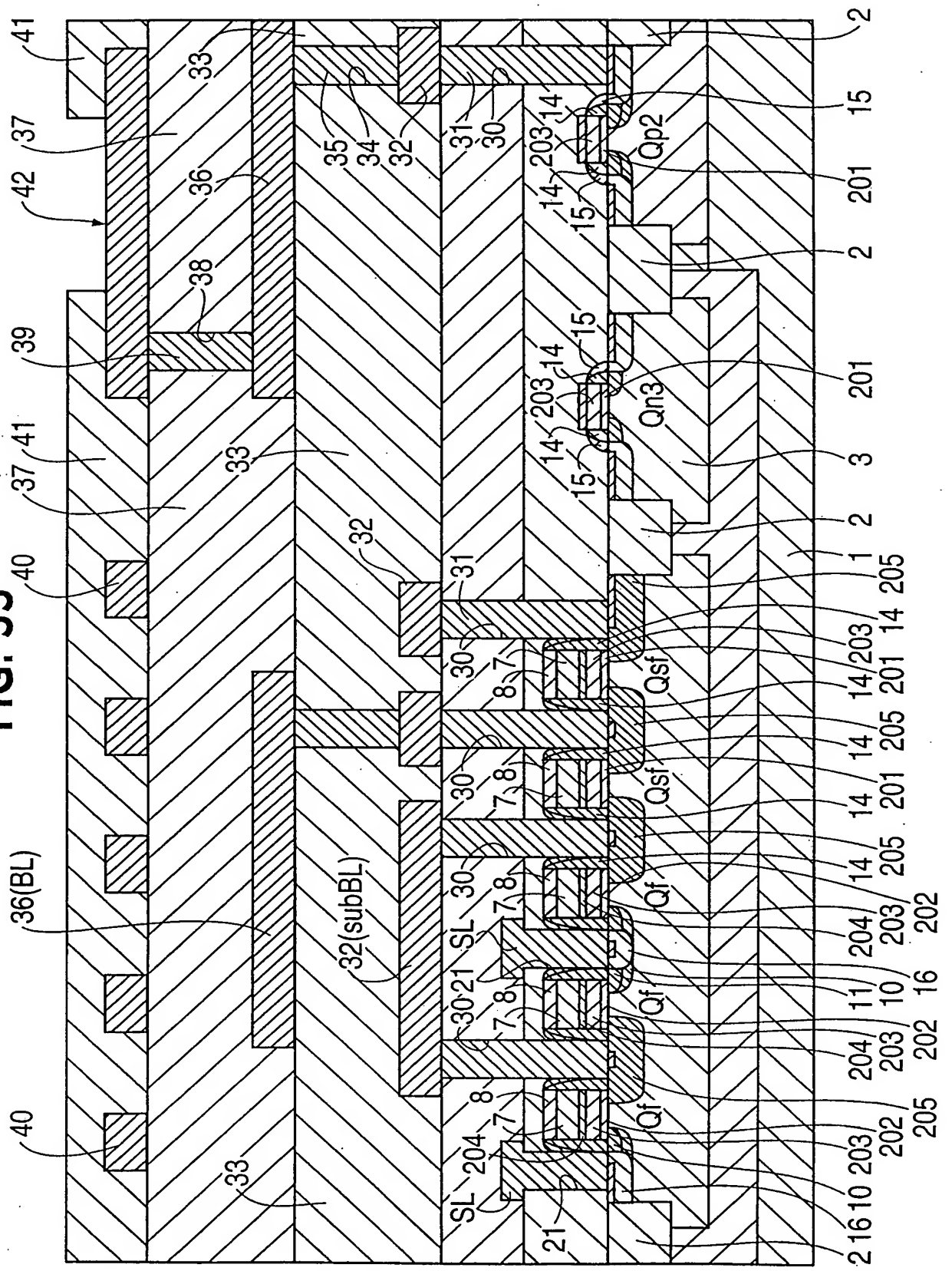


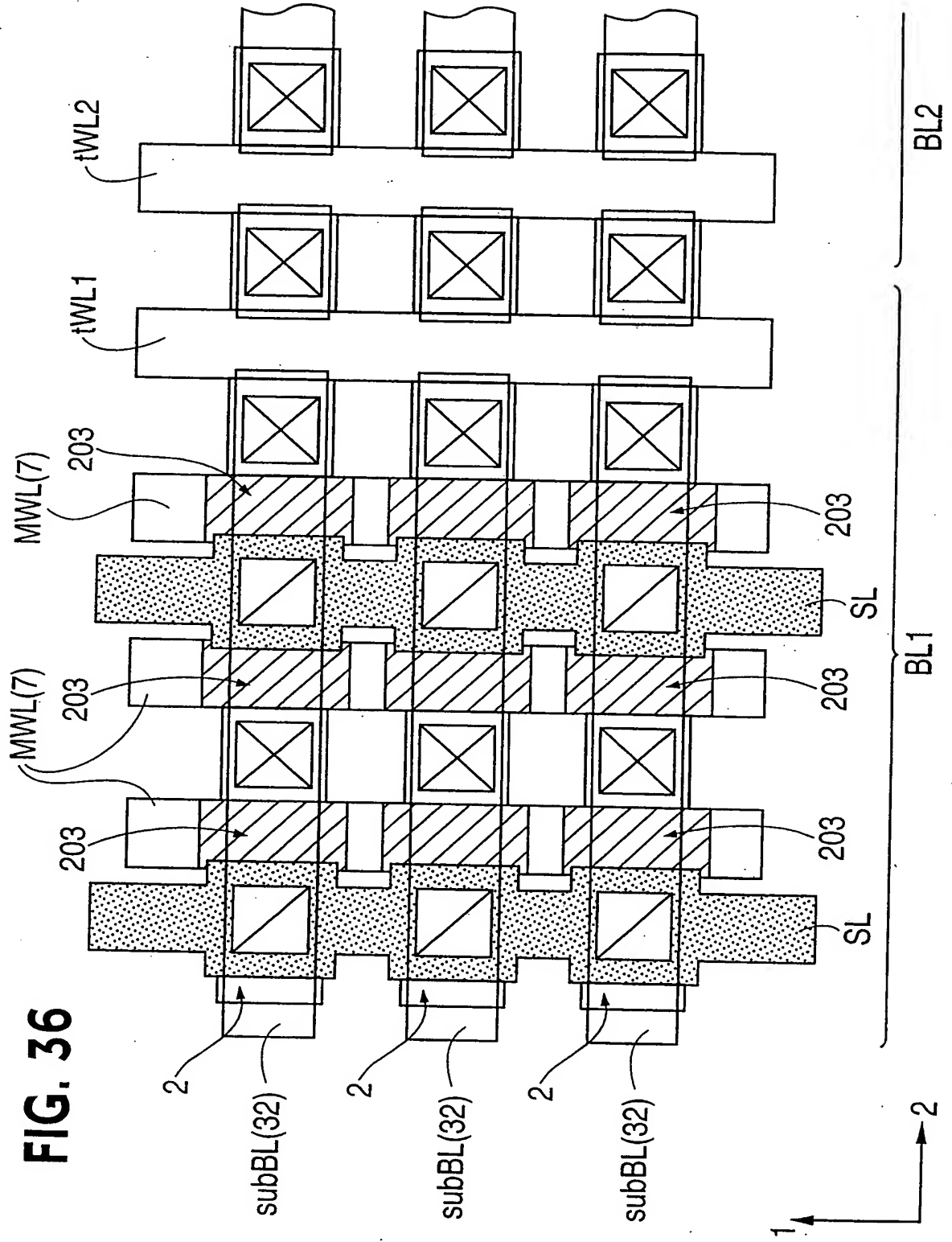
FIG. 34



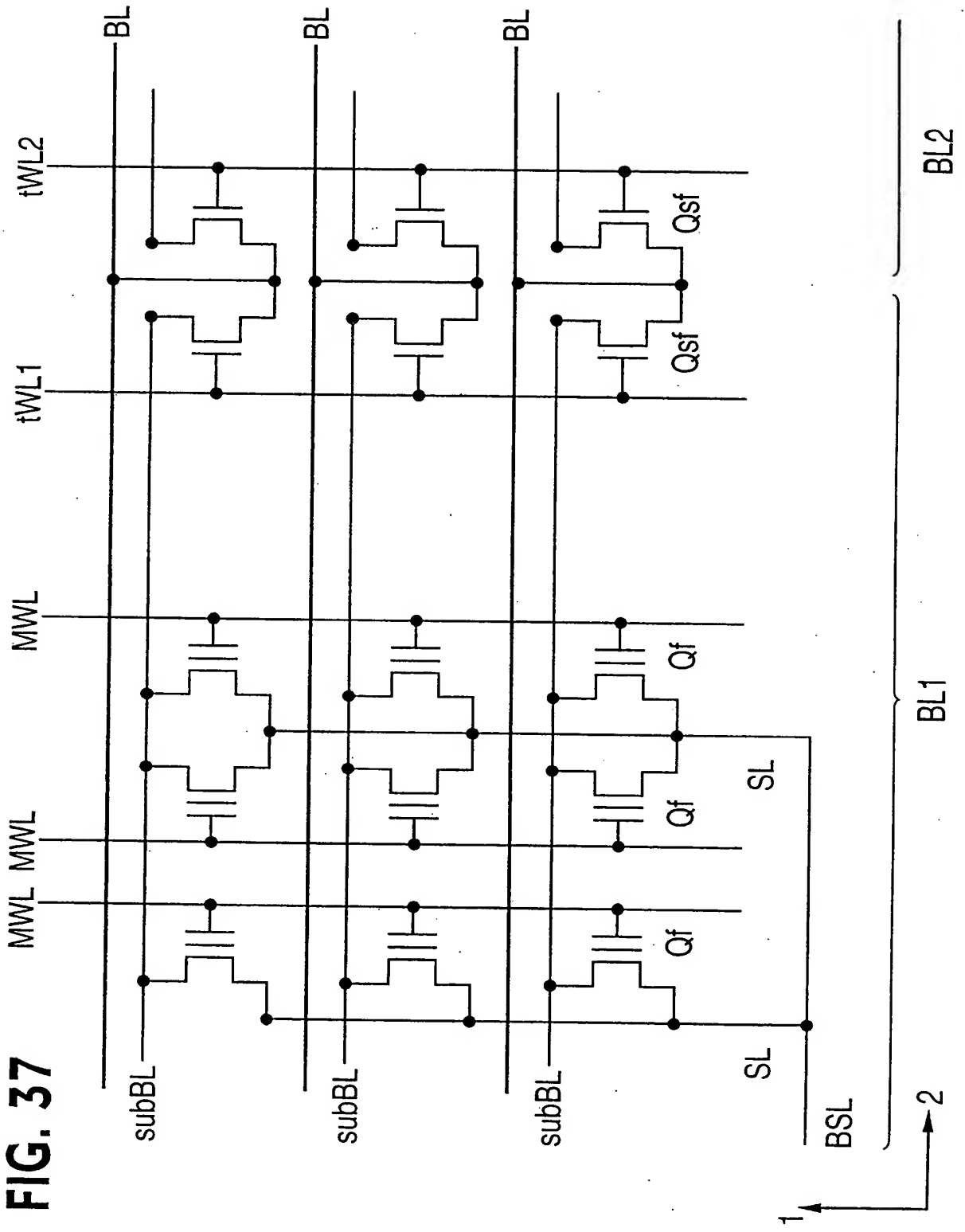
**FIG. 35**



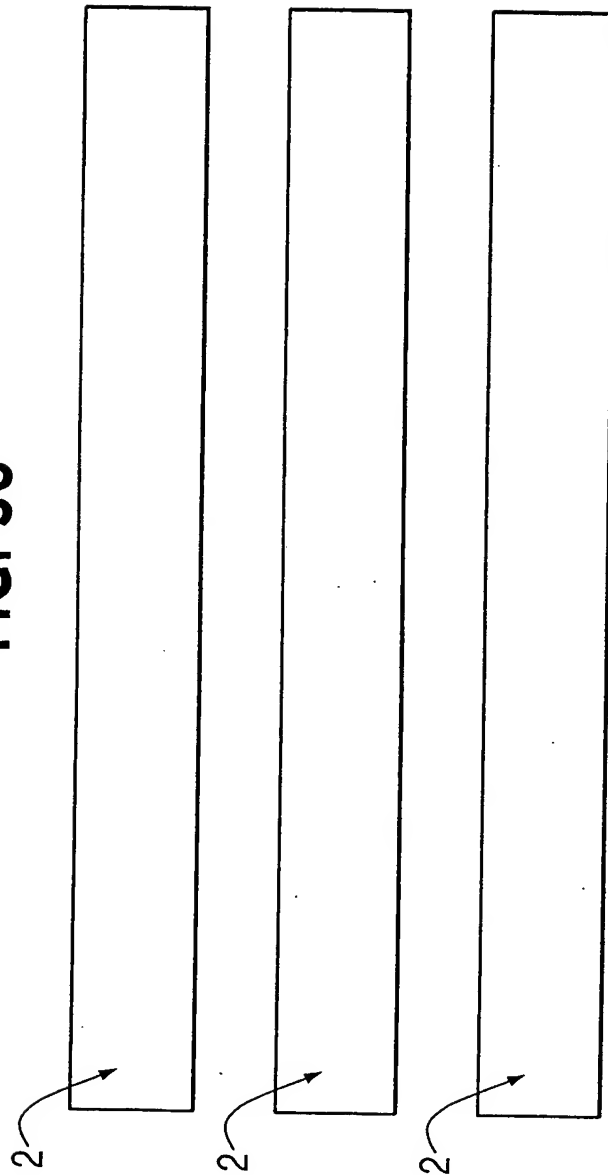
**FIG. 36**



**FIG. 37**



**FIG. 38**





**FIG. 40**

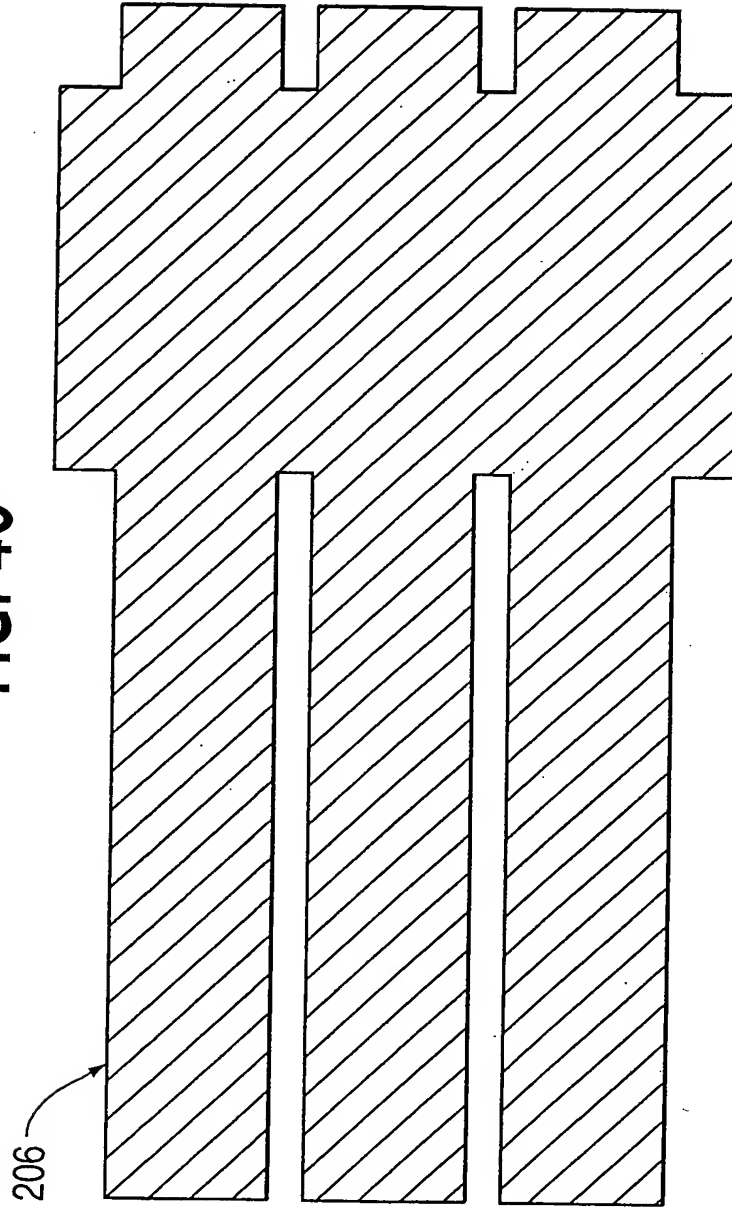




FIG. 41

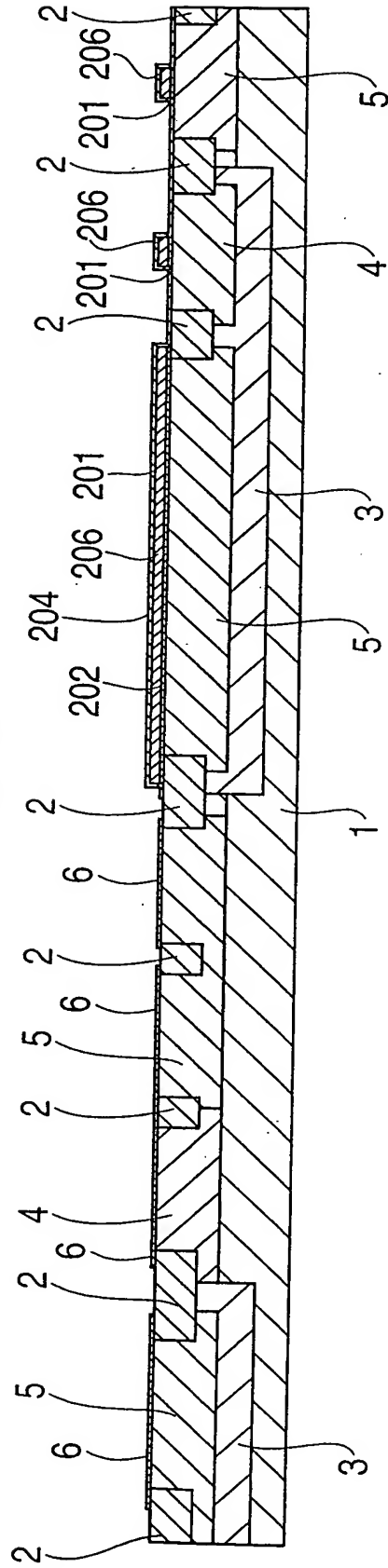
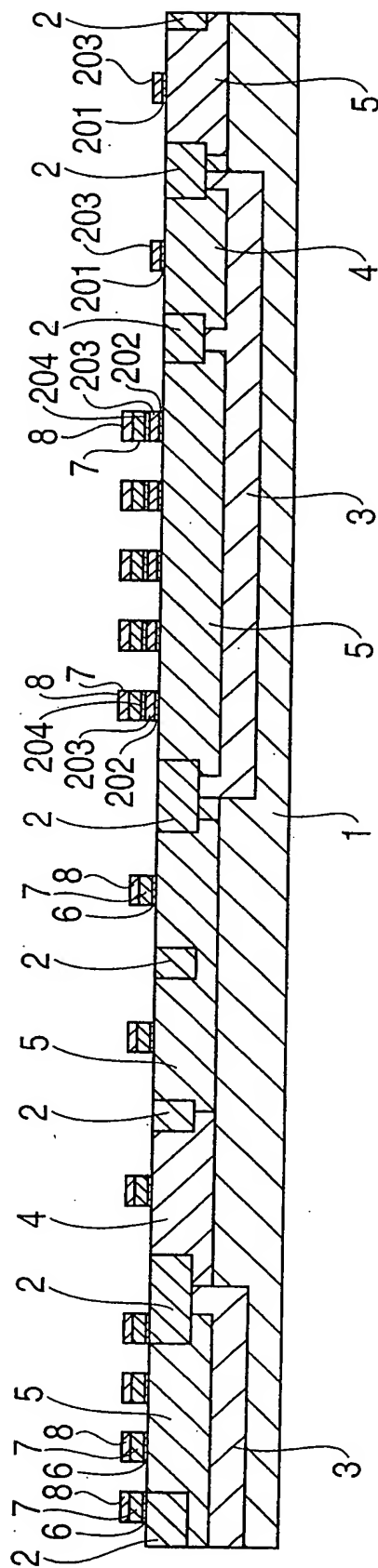
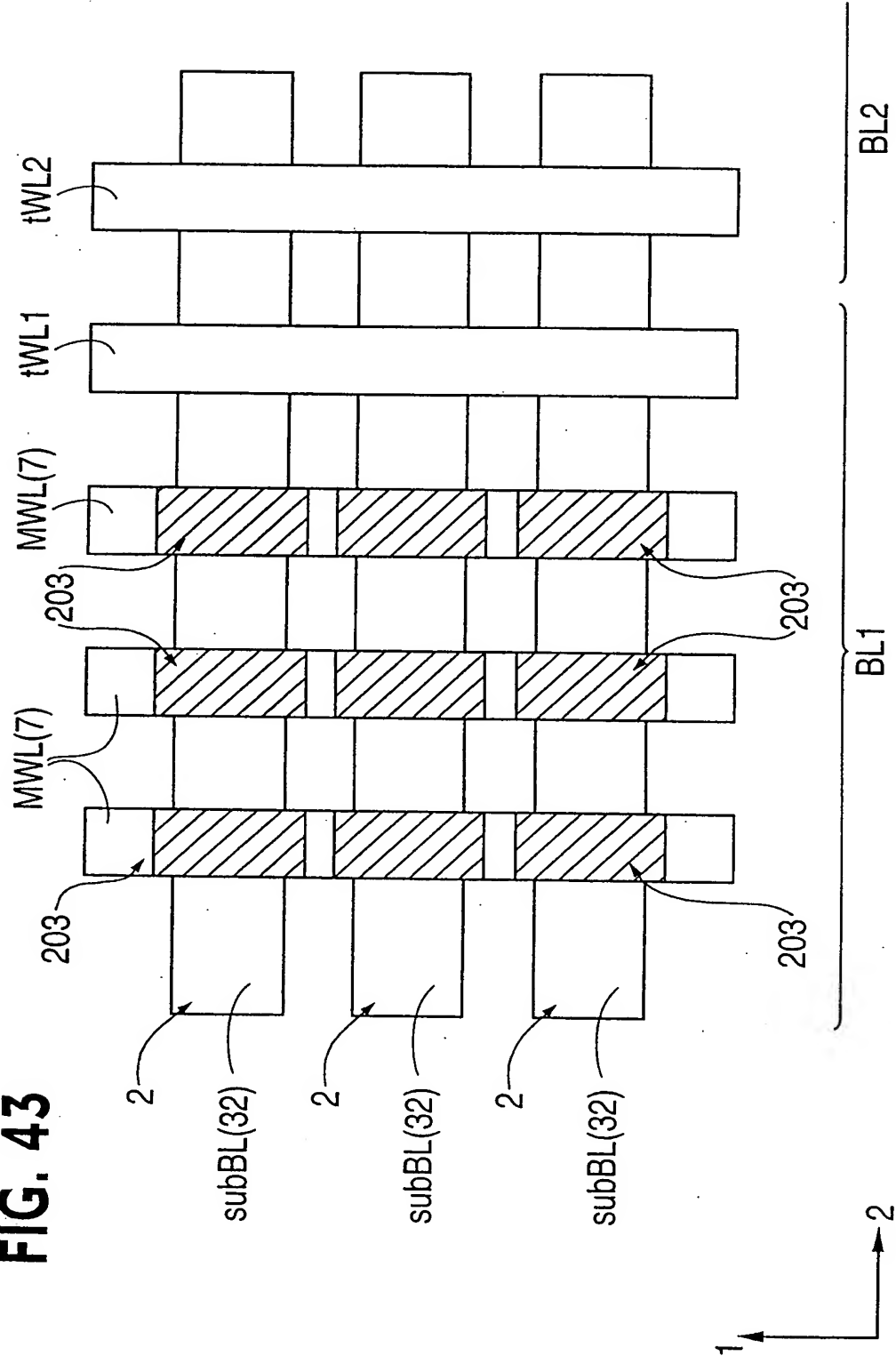


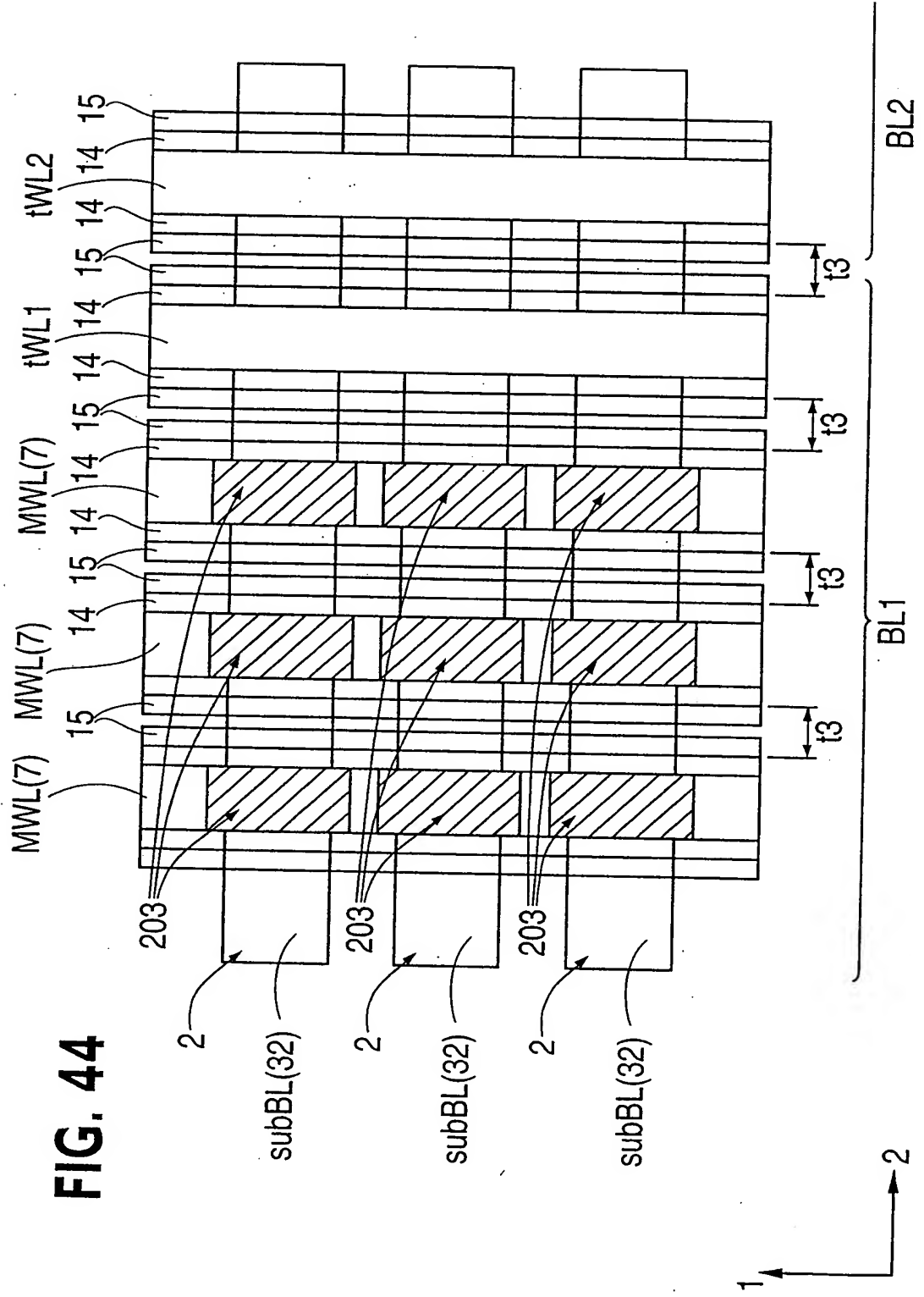
FIG. 42

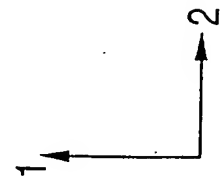


**FIG. 43**



**FIG. 44**



[illegible]

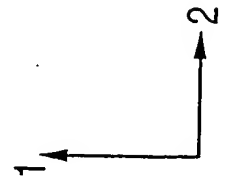


FIG. 47

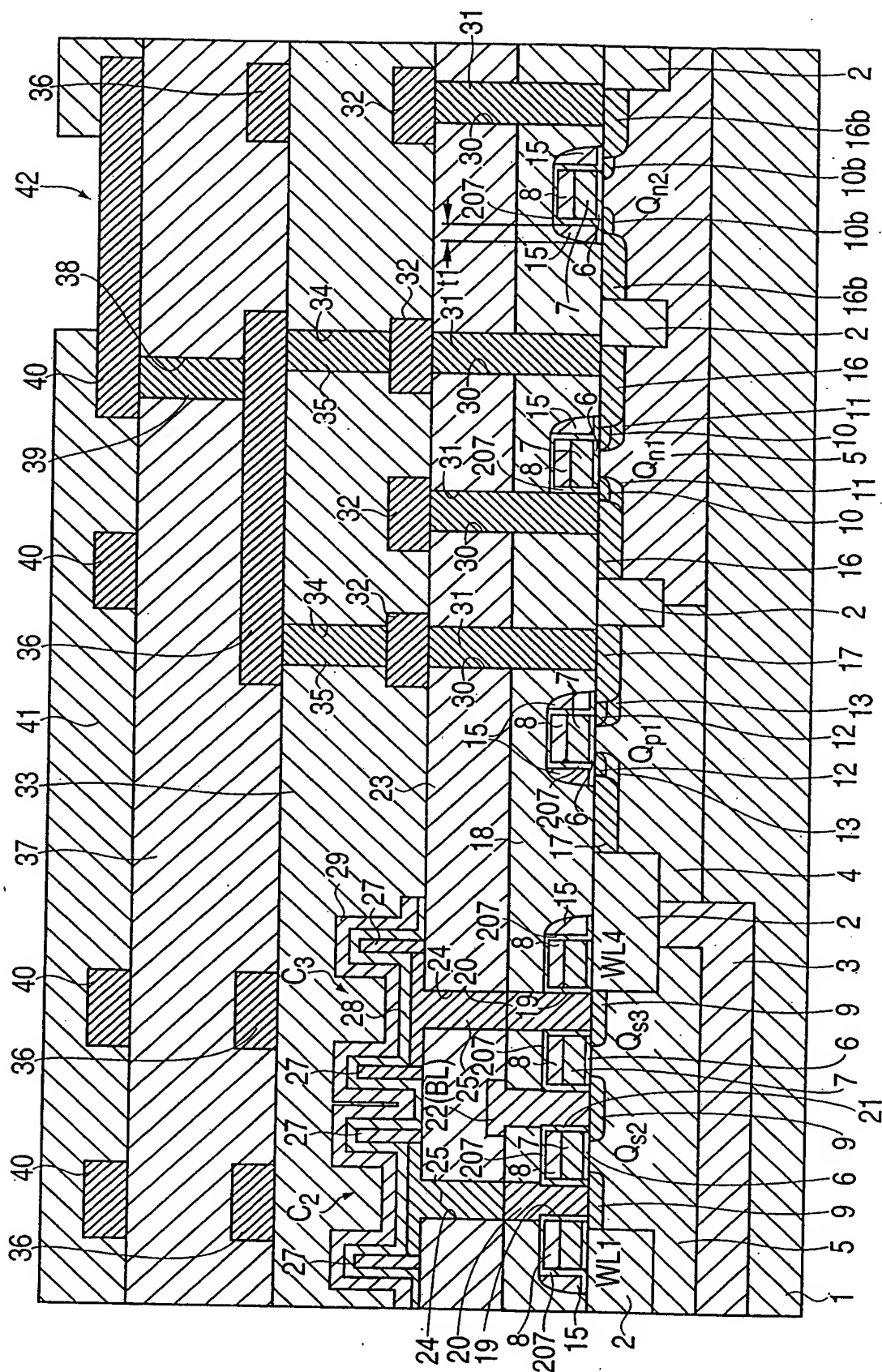


FIG. 48

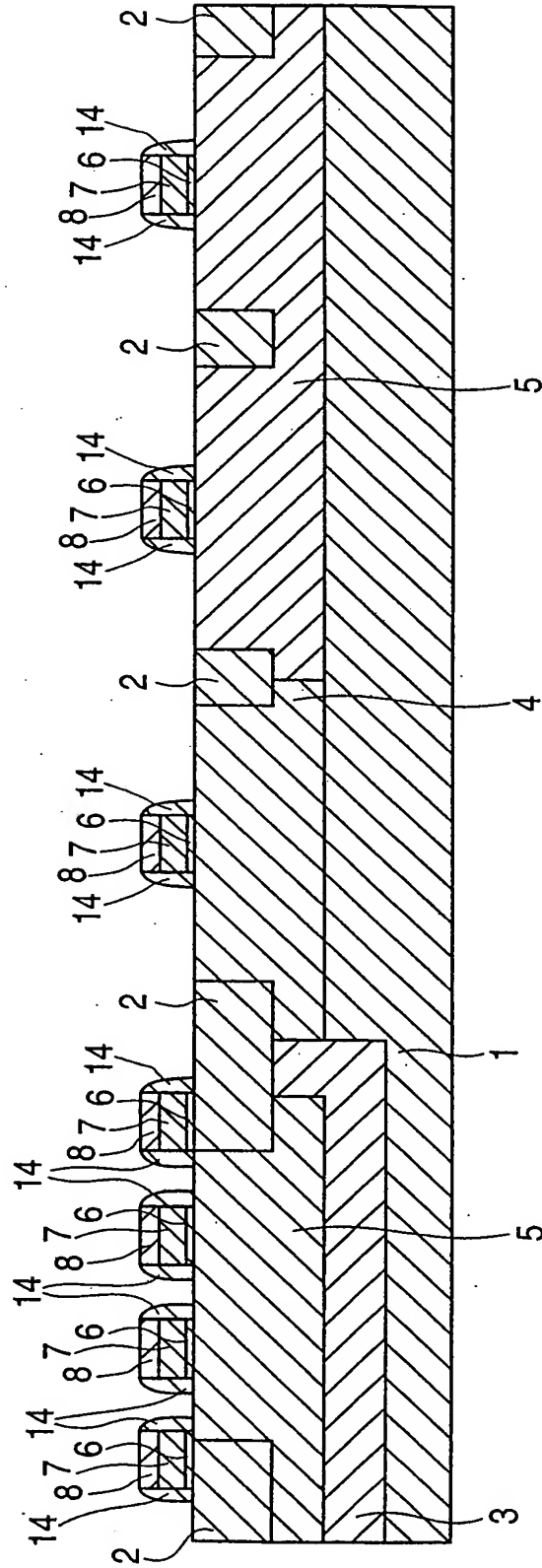




FIG. 49

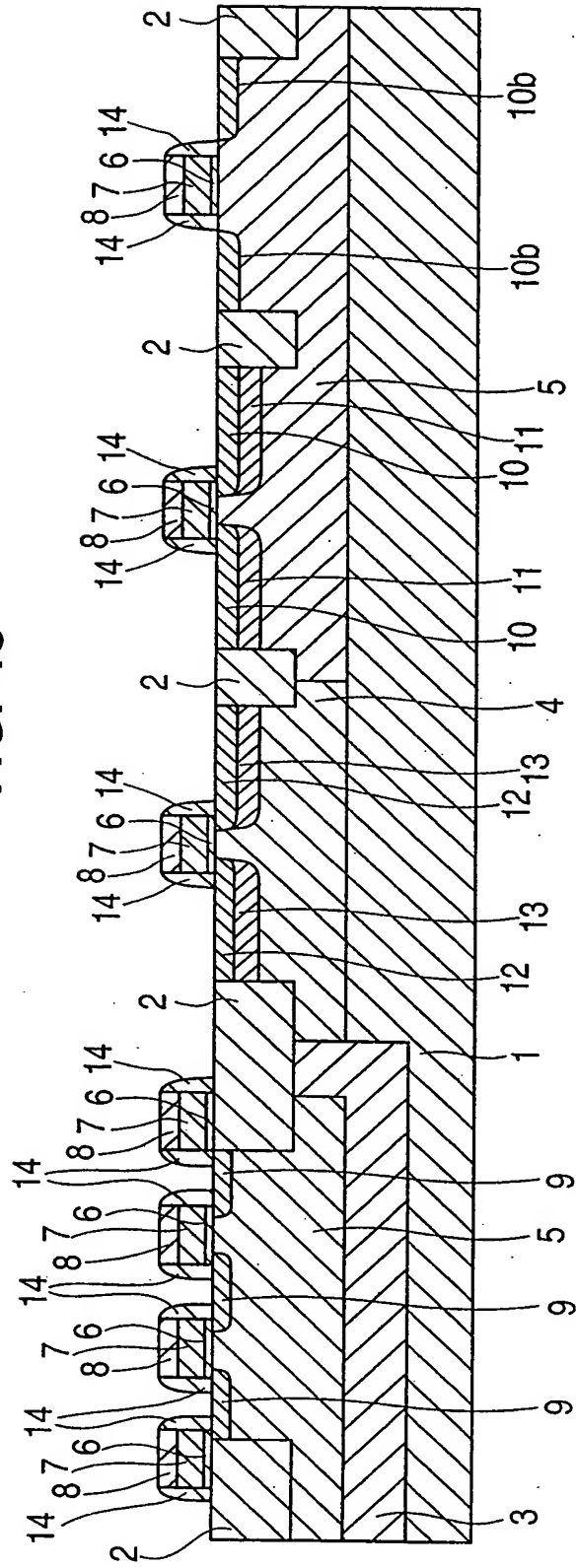


FIG. 50(a)

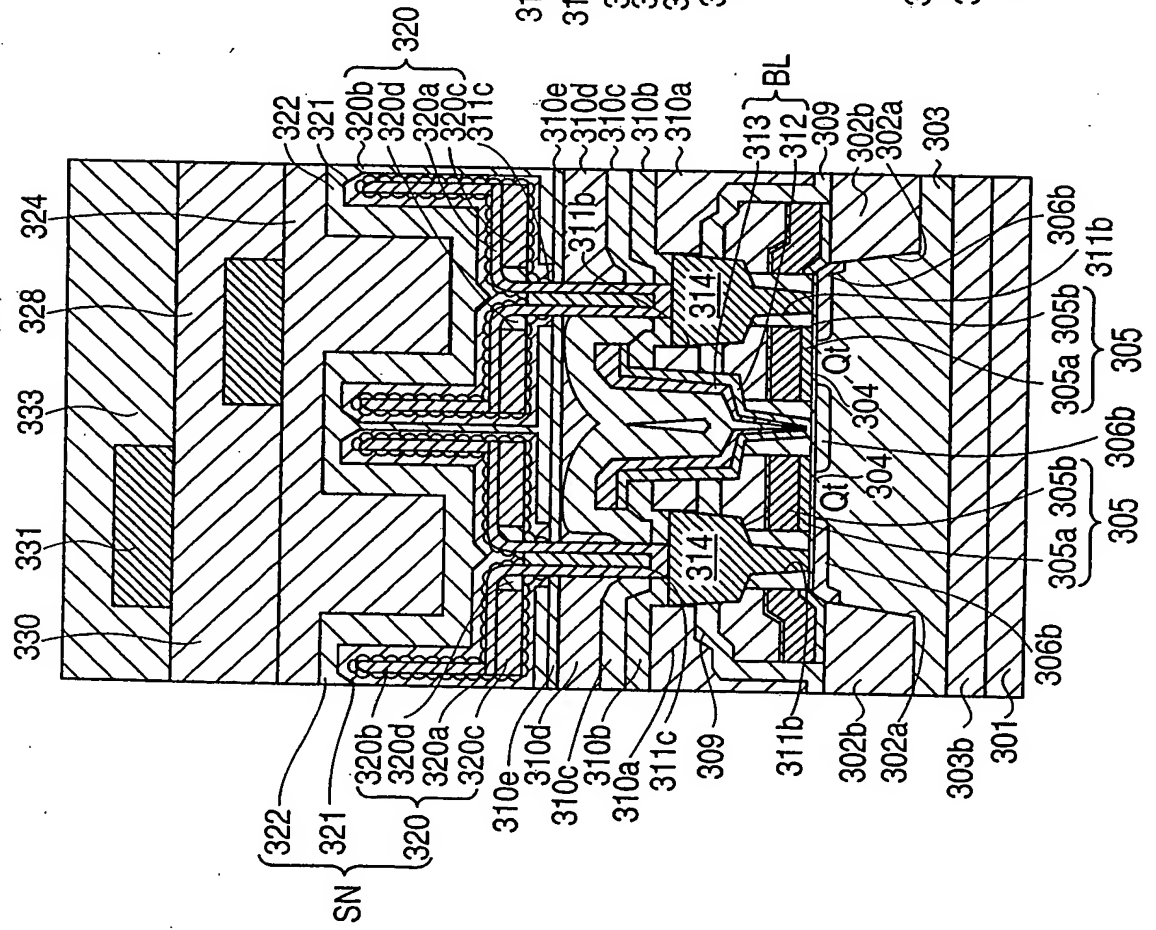
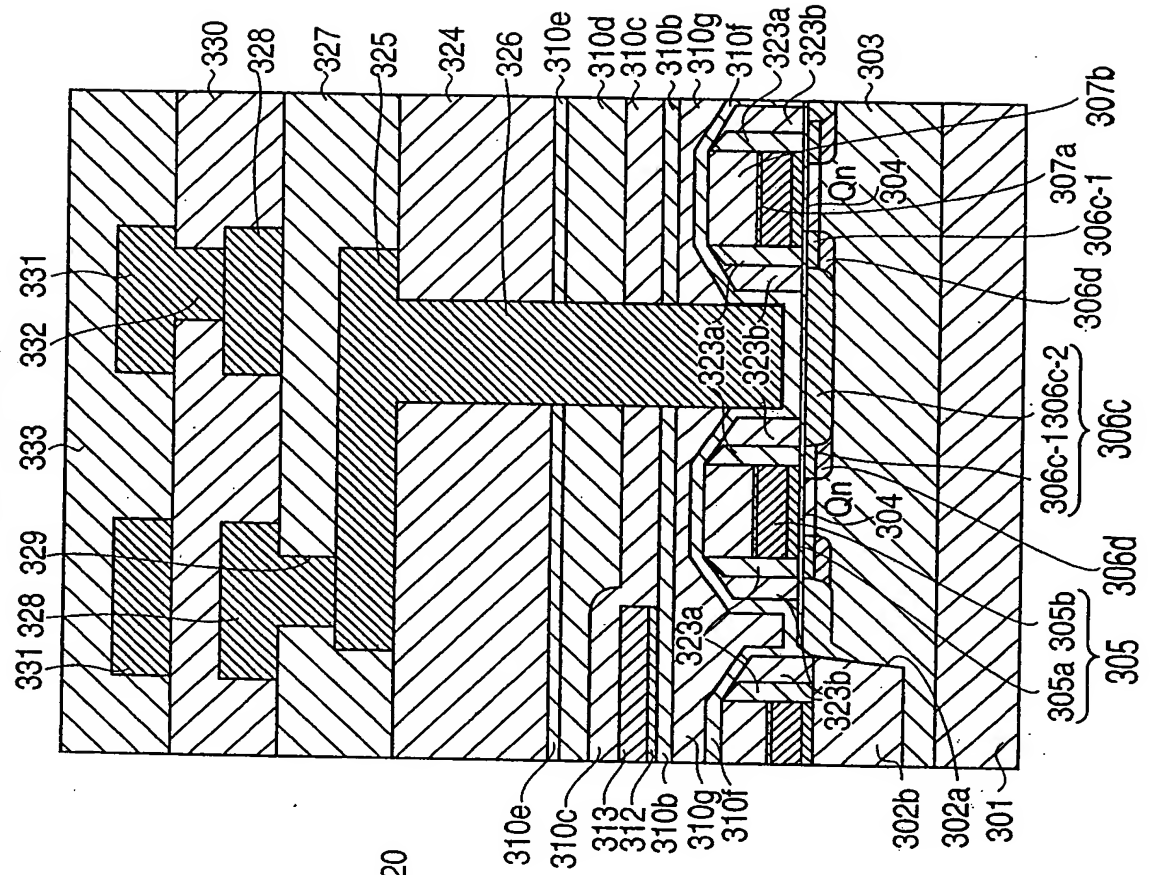


FIG. 50(b)



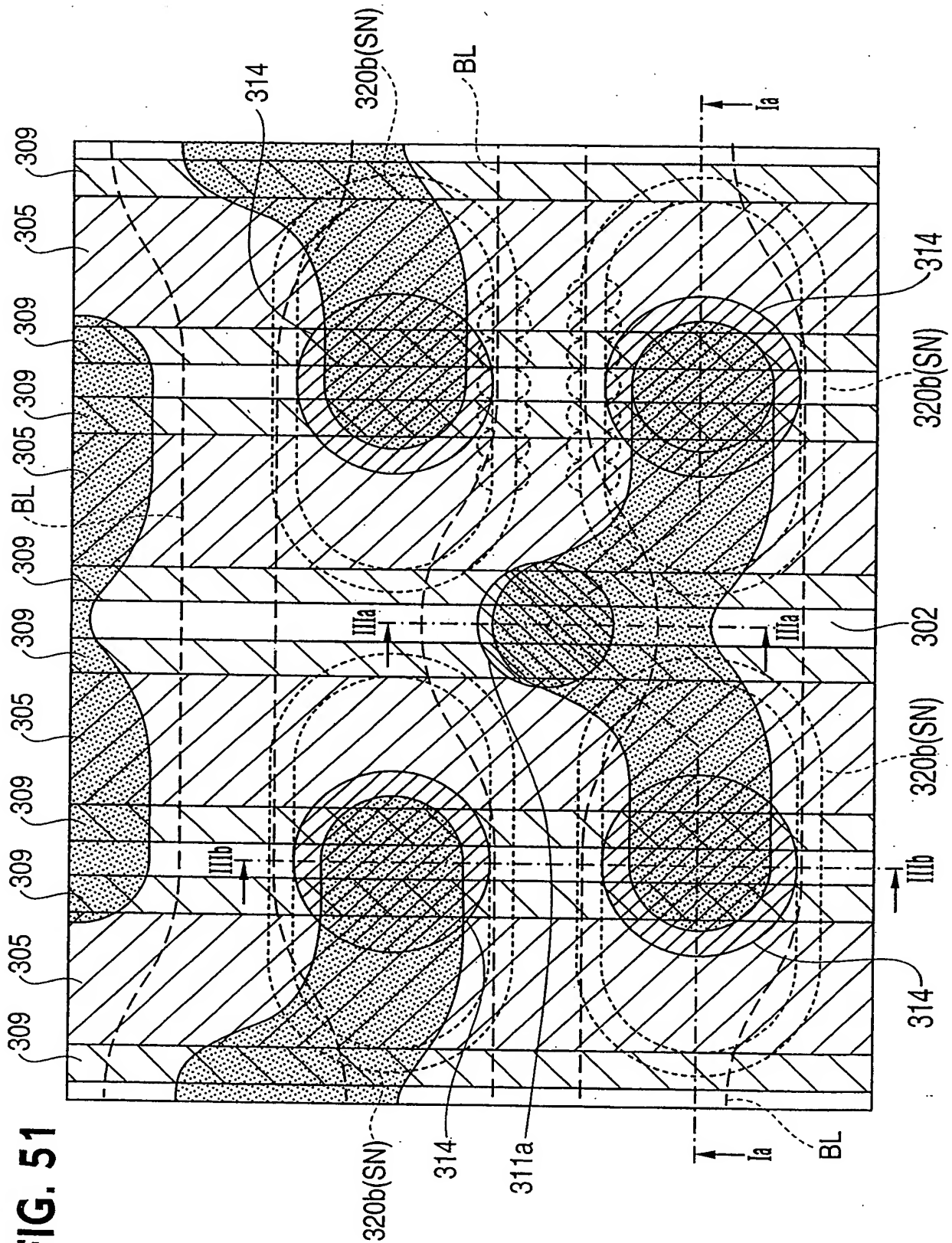


FIG. 52(a)

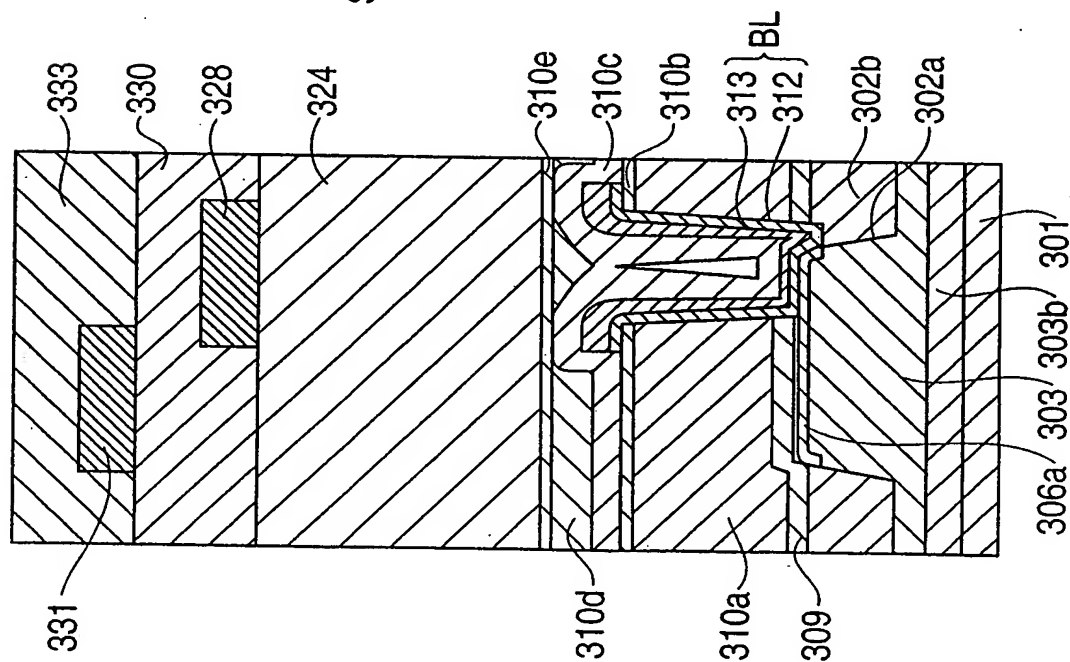
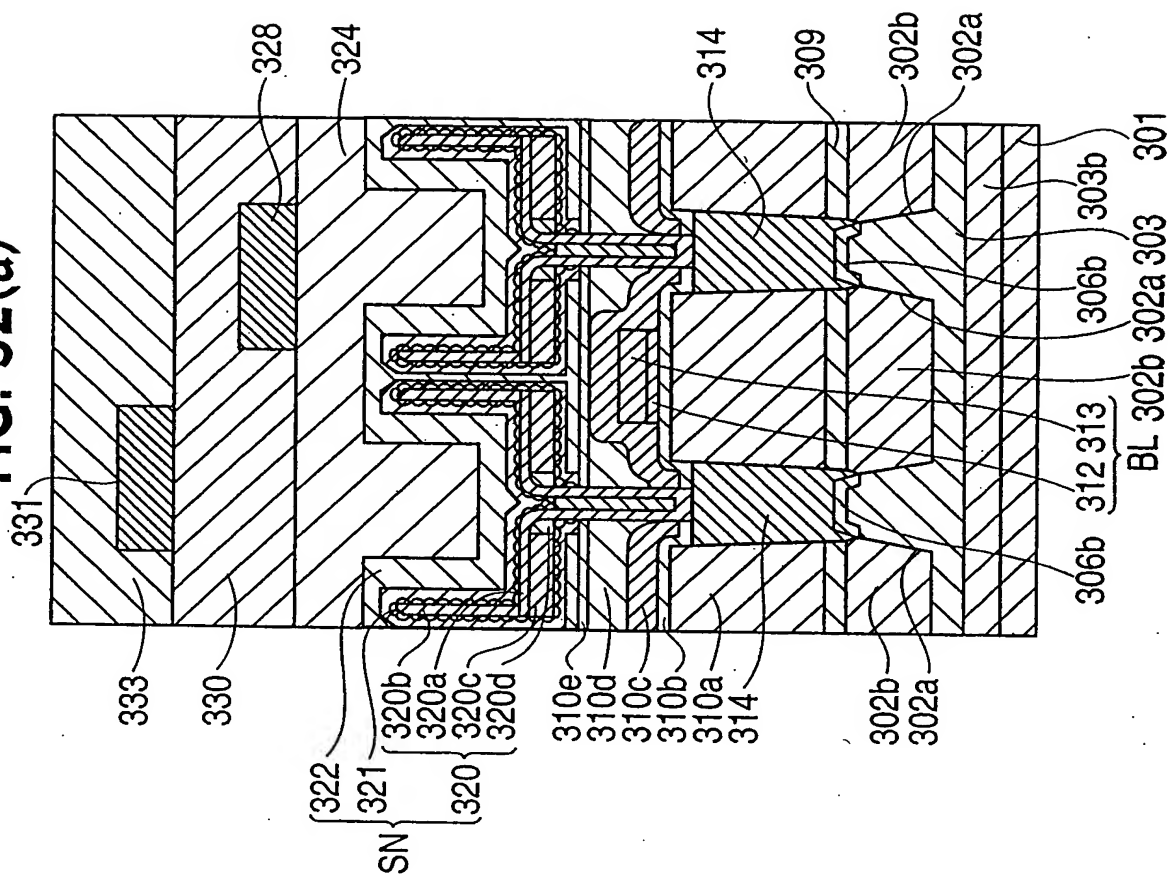
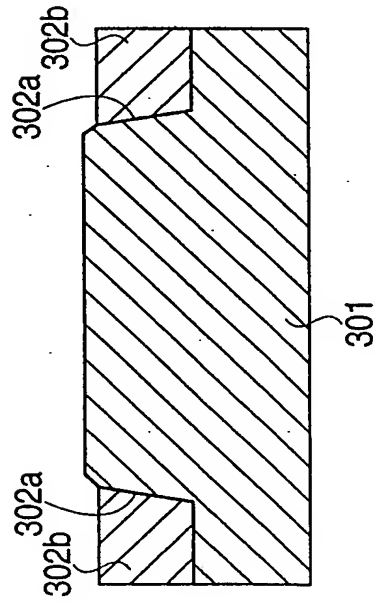


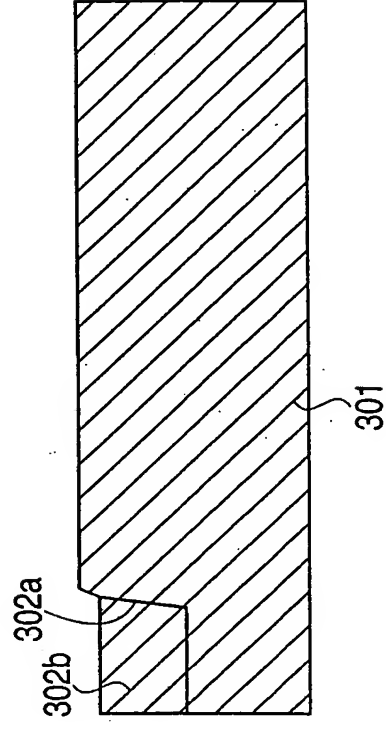
FIG. 52(a)



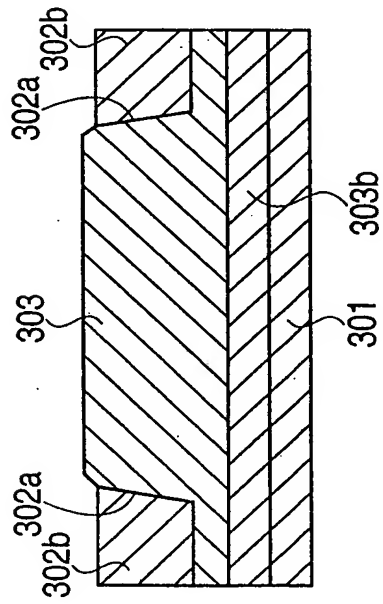
**FIG. 53(a)**



**FIG. 53(b)**



**FIG. 54(a)**



**FIG. 54(b)**

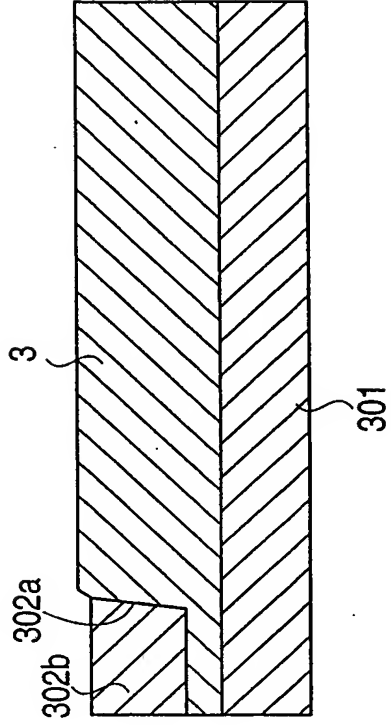


FIG. 55(a)

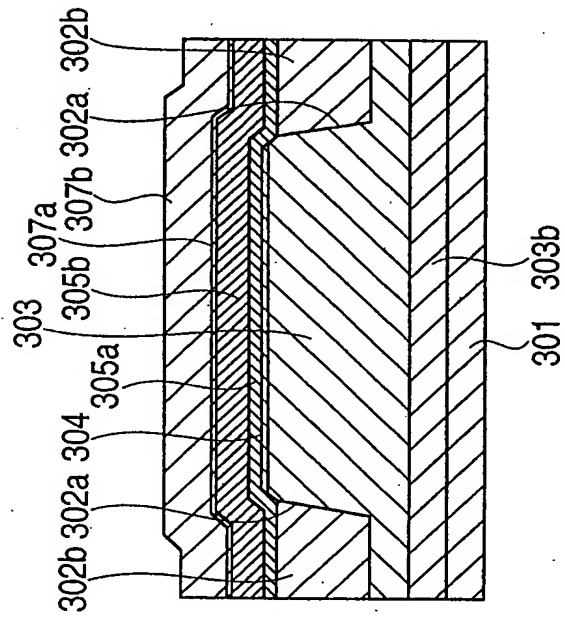
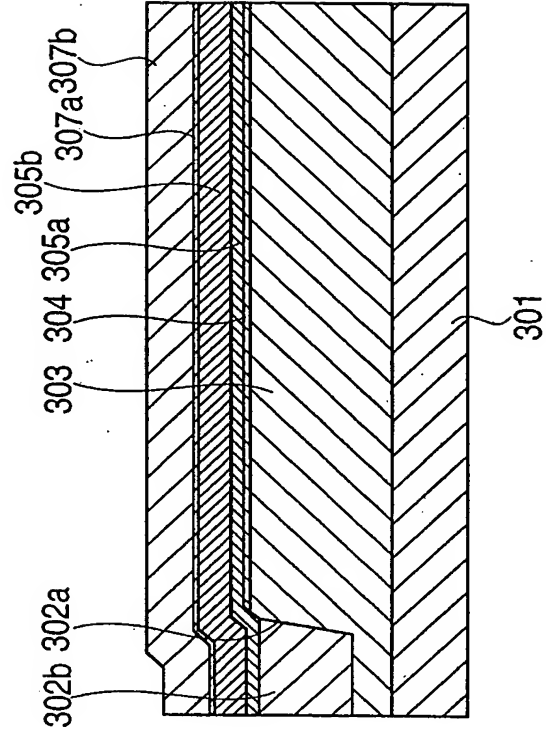
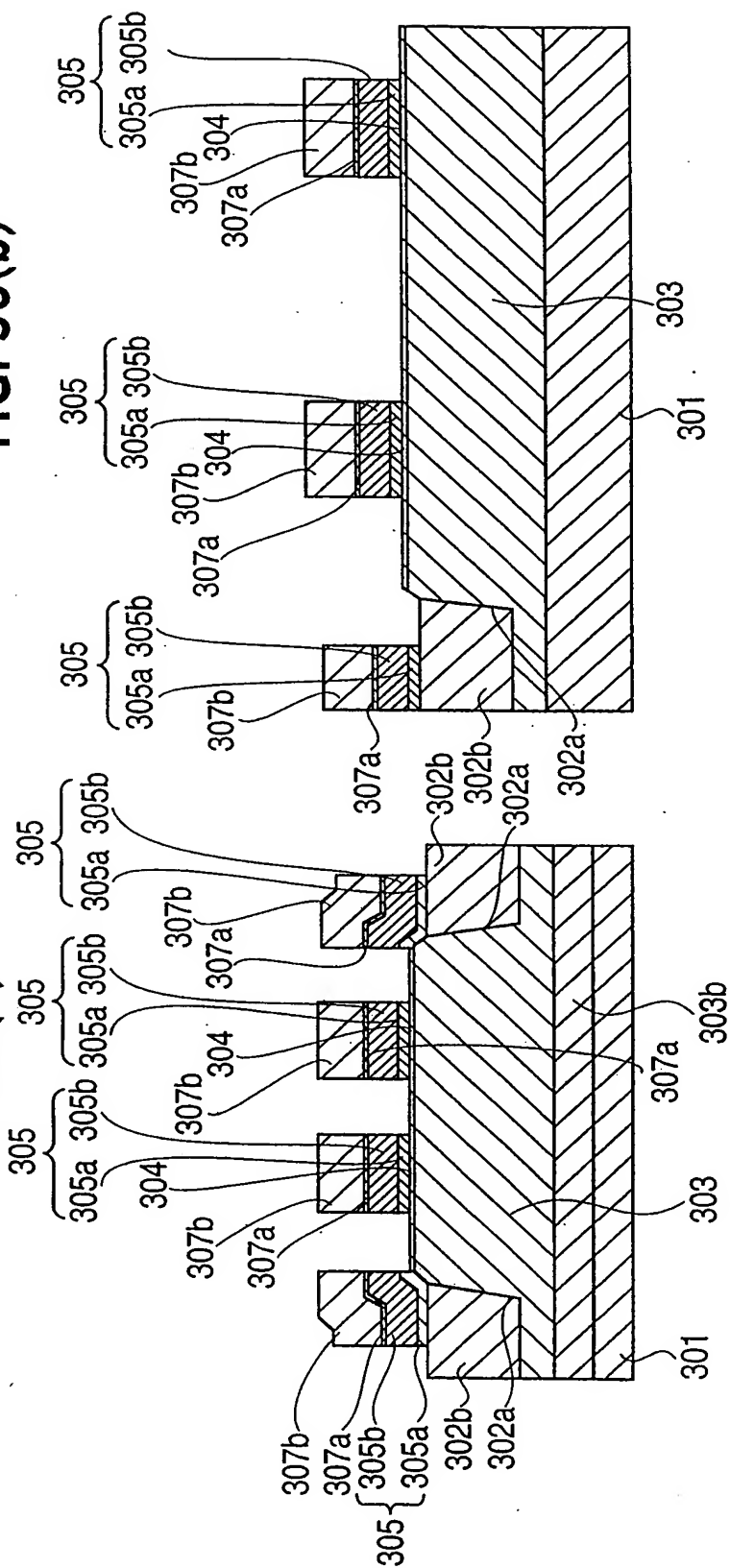


FIG. 55(b)

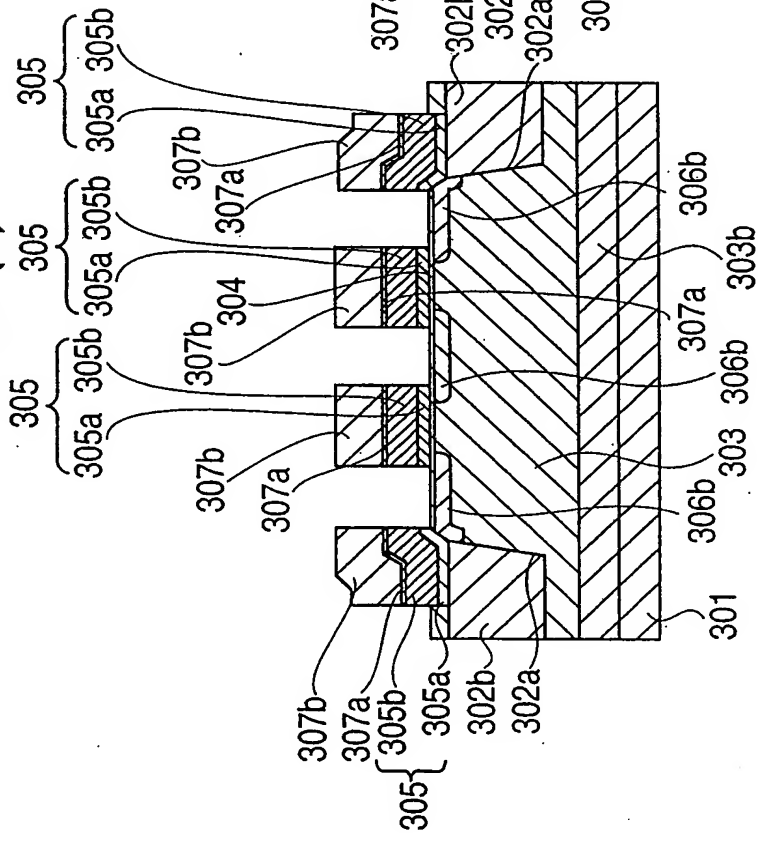


**FIG. 56(b)**

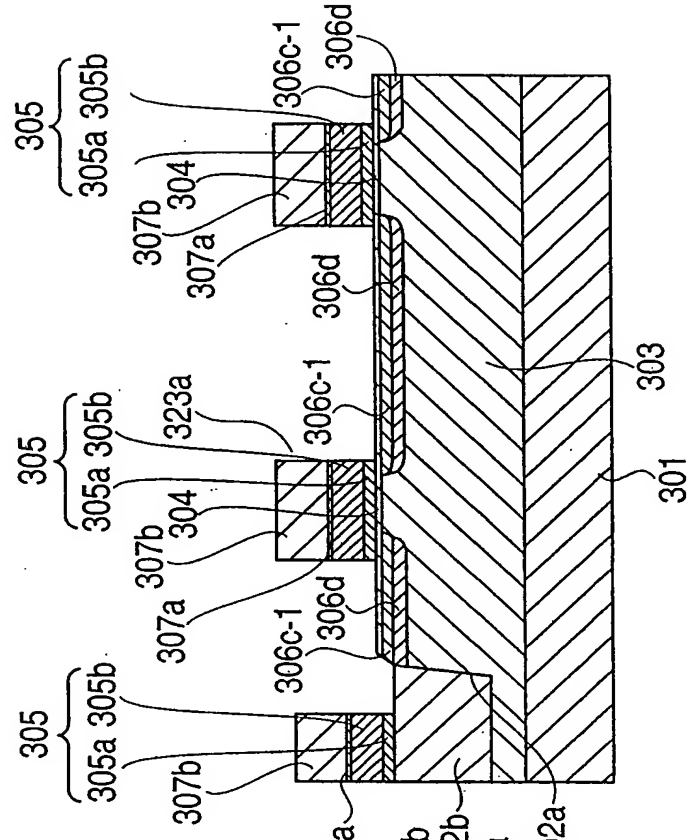




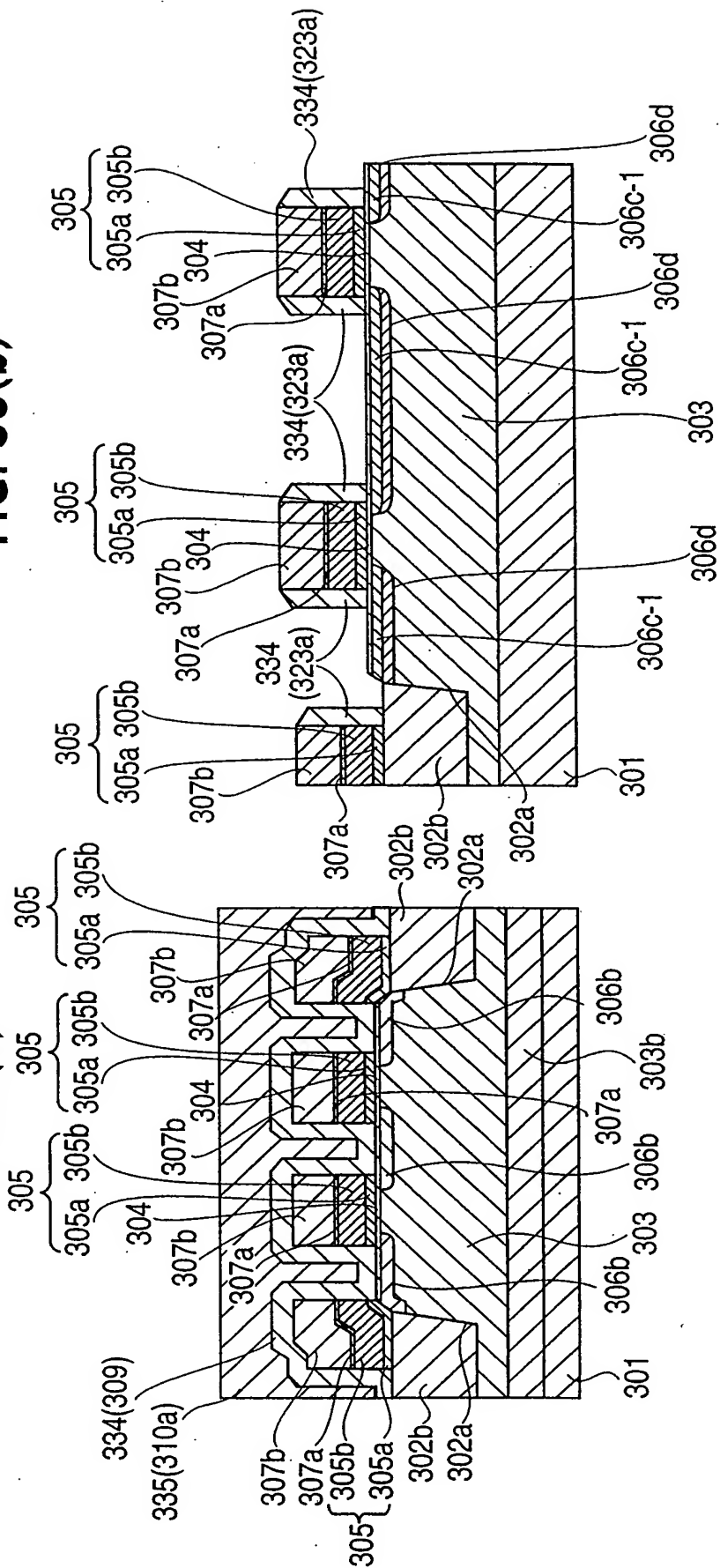
**FIG. 57(a)**



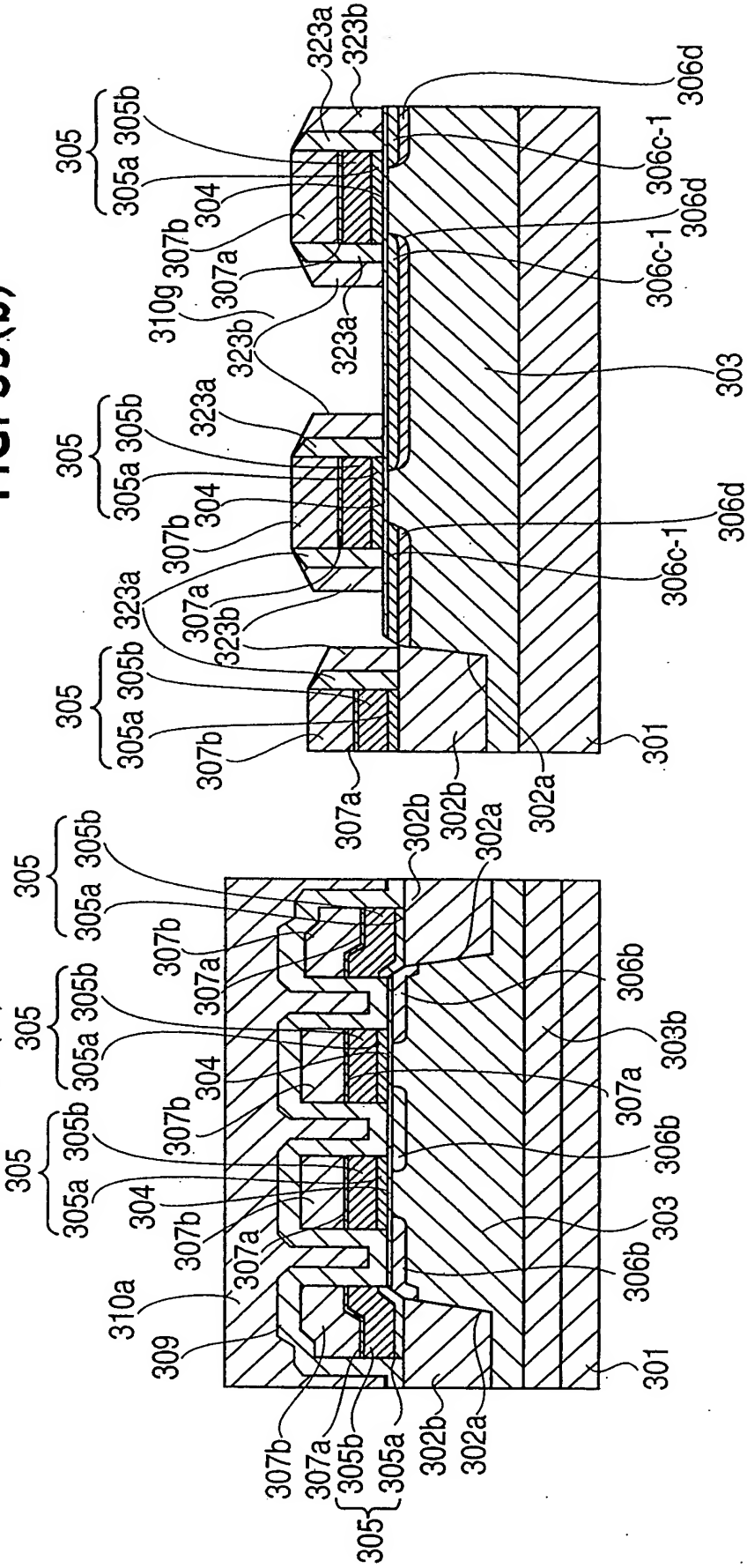
**FIG. 57(b)**



**FIG. 58(b)**

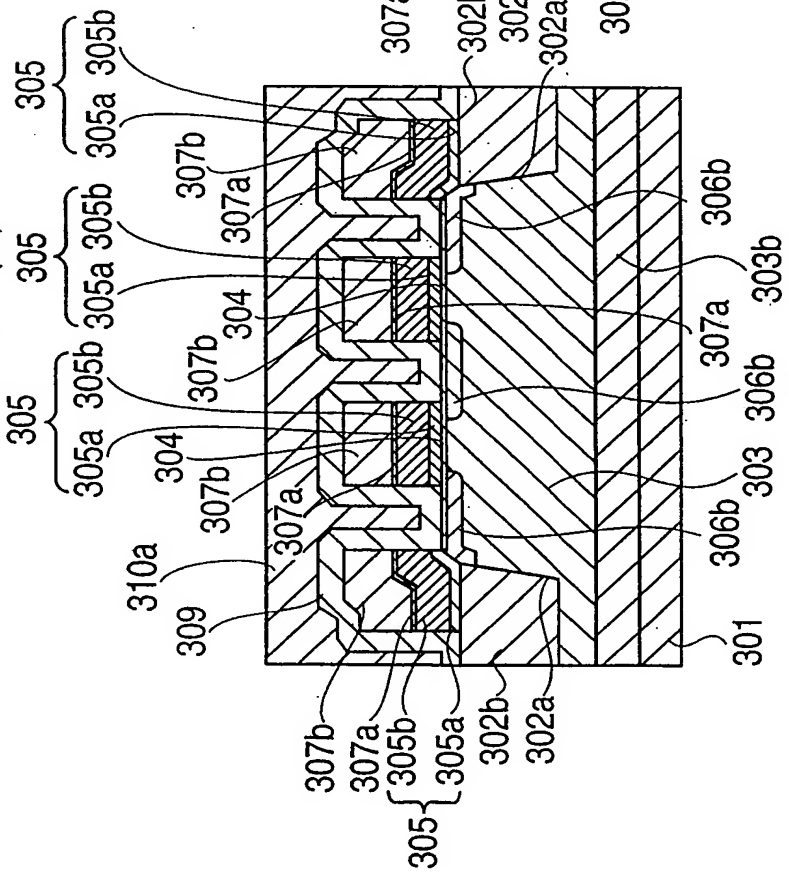


**FIG. 59(b)**

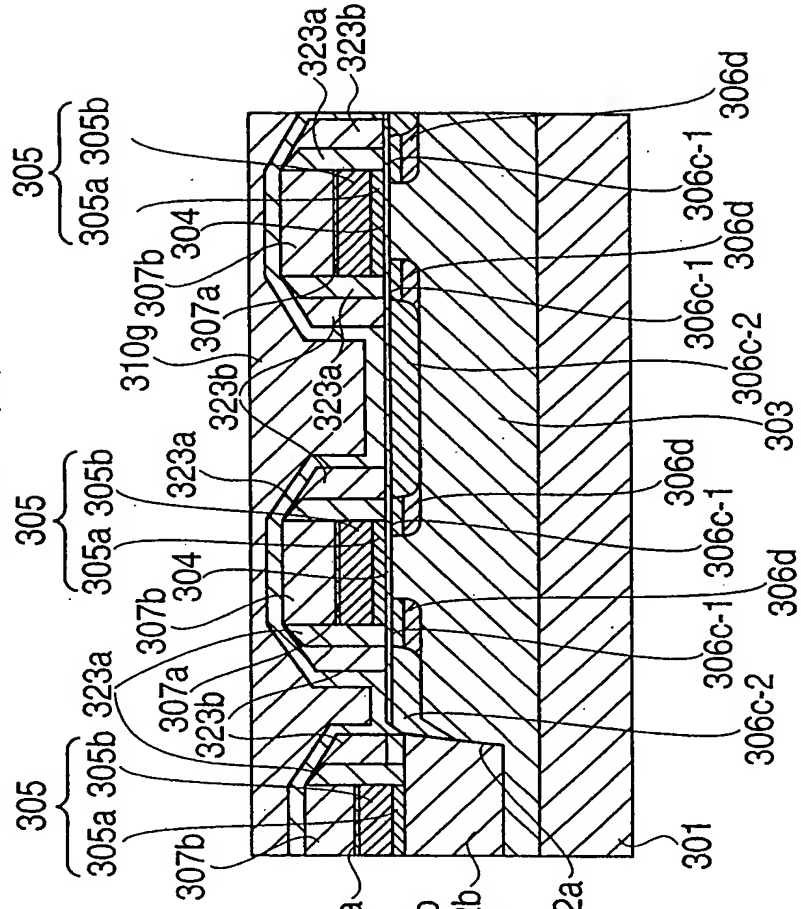




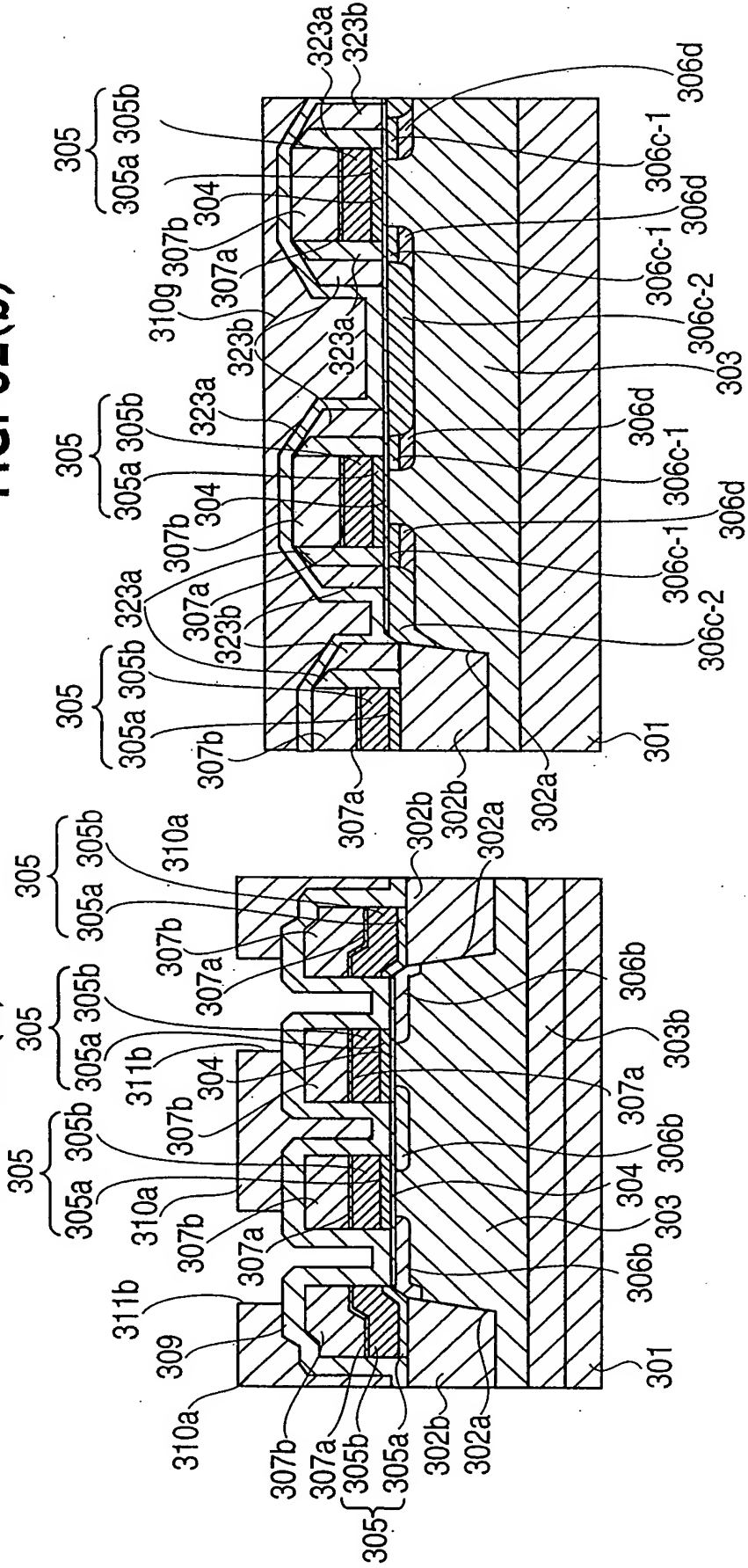
**FIG. 61(a)**



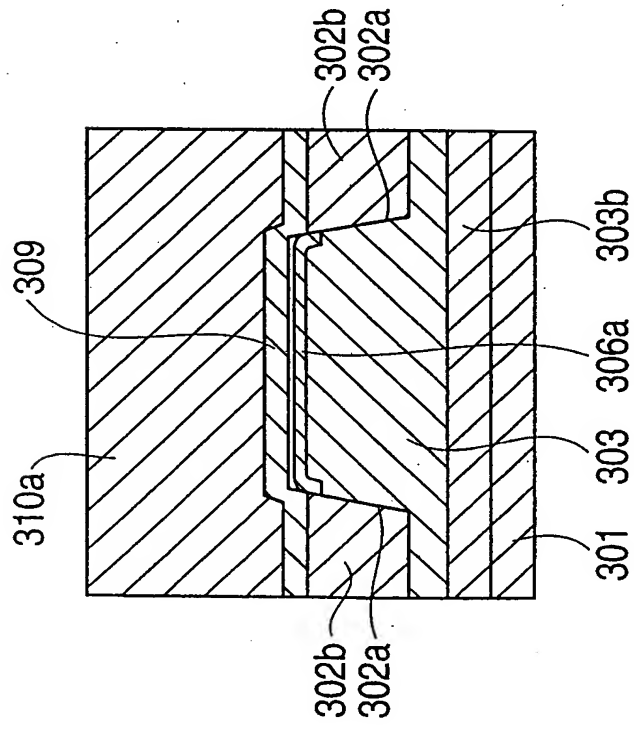
**FIG. 61(b)**



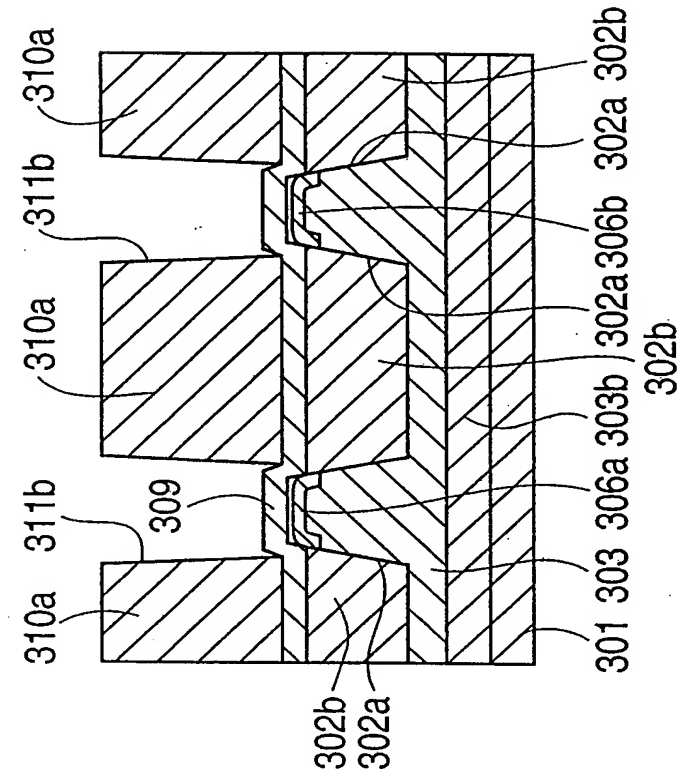
**FIG. 62(b)**



**FIG. 63(a)**



**FIG. 63(b)**



**FIG. 64(b)**





FIG. 65(a)

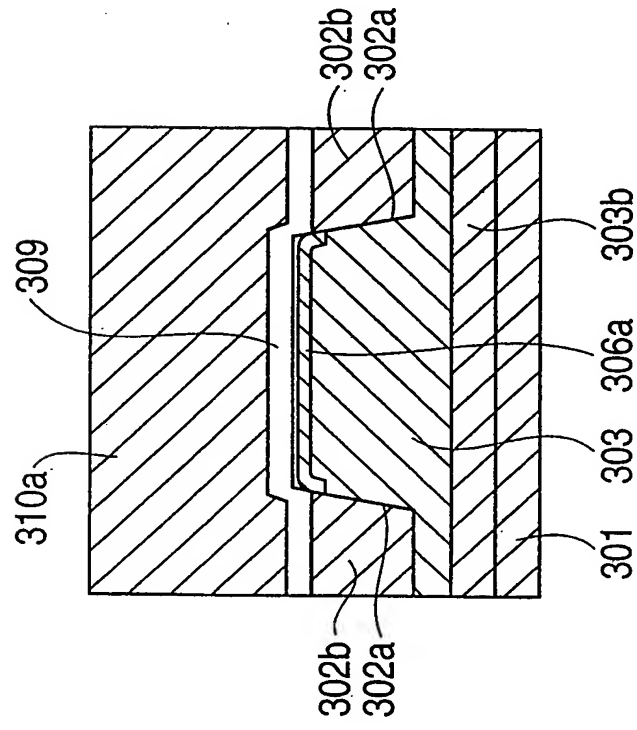
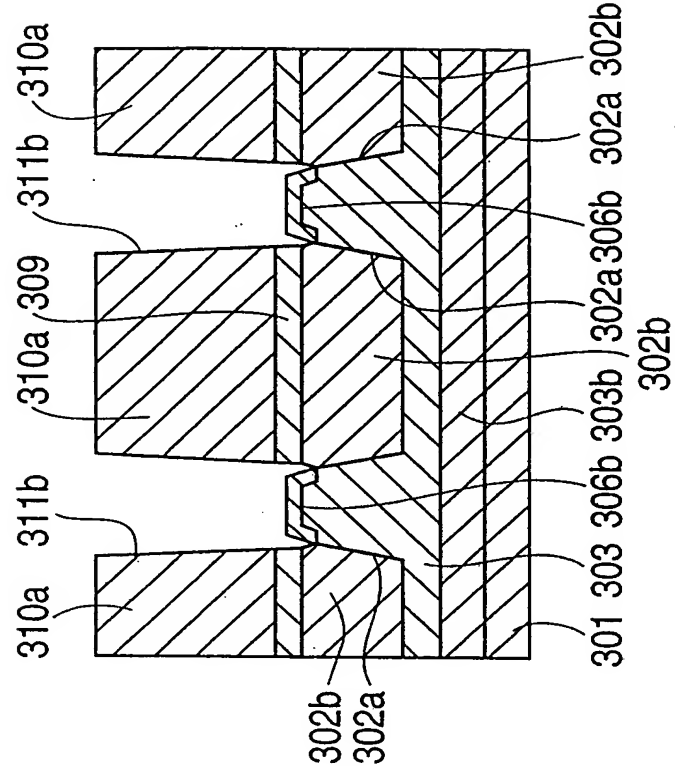
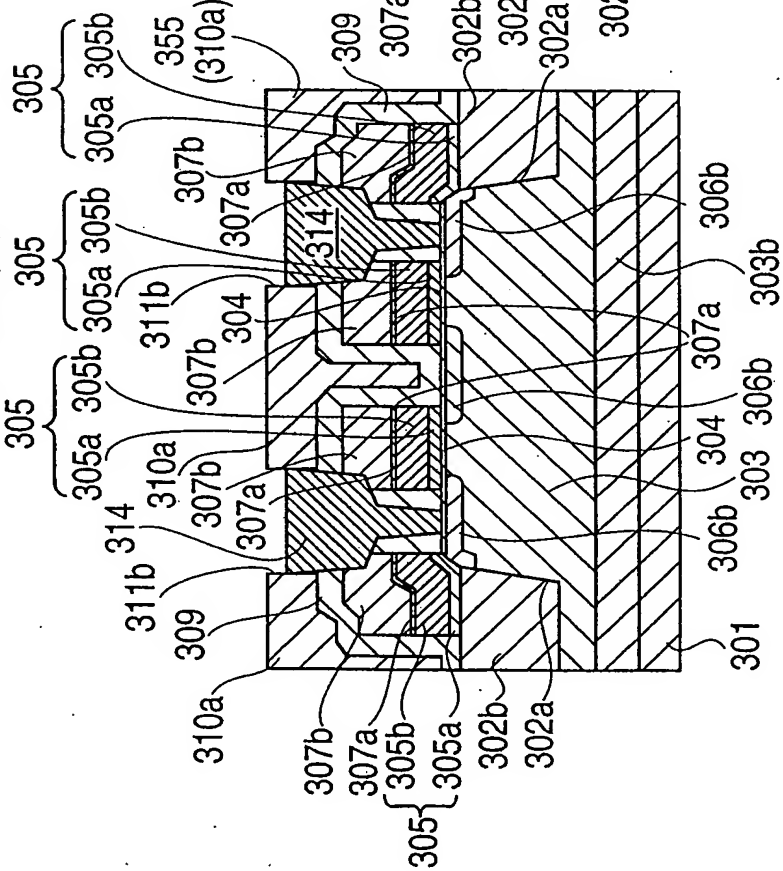


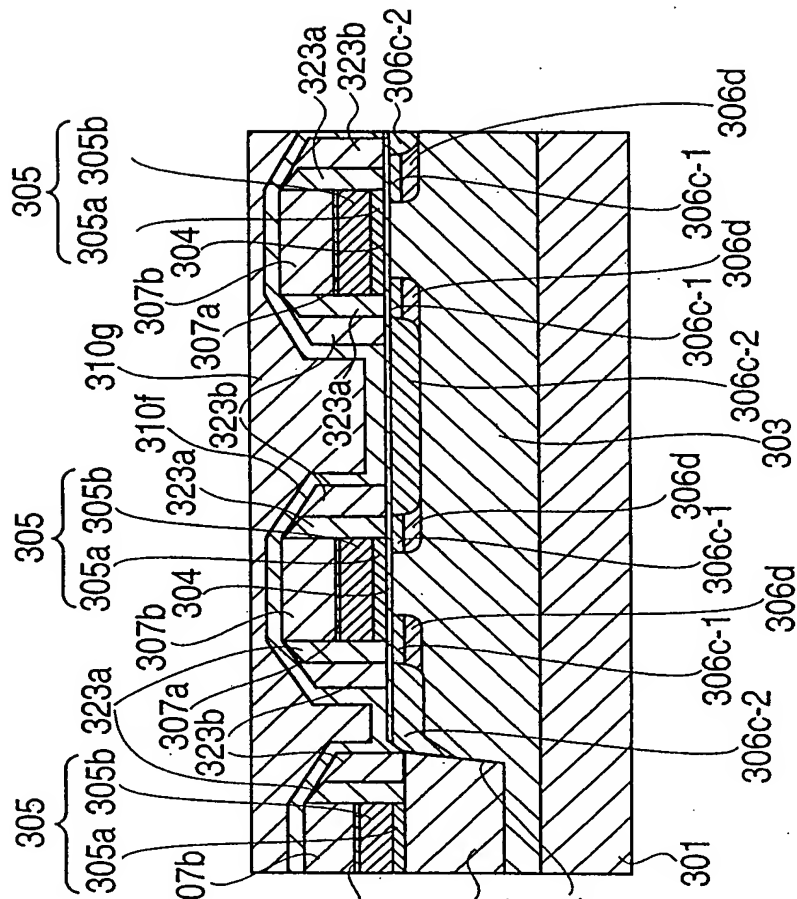
FIG. 65(b)



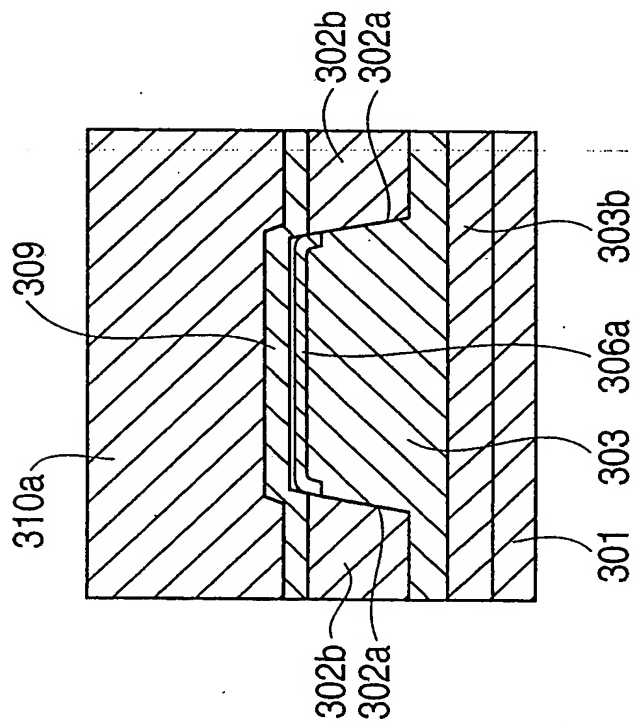
**FIG. 66(a)**



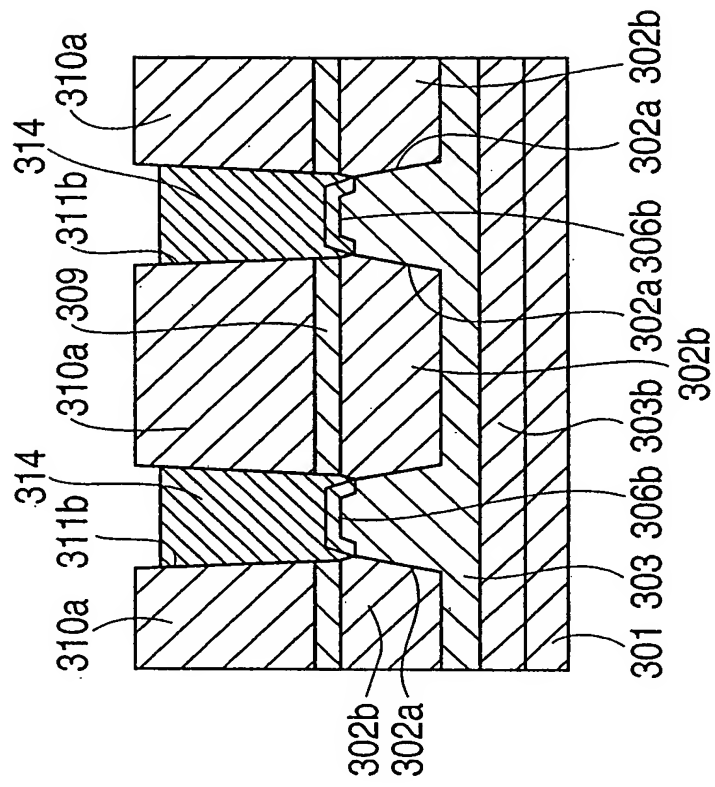
**FIG. 66(b)**



**FIG. 67(a)**



**FIG. 67(b)**



**FIG. 68(b)**



FIG. 69(a)

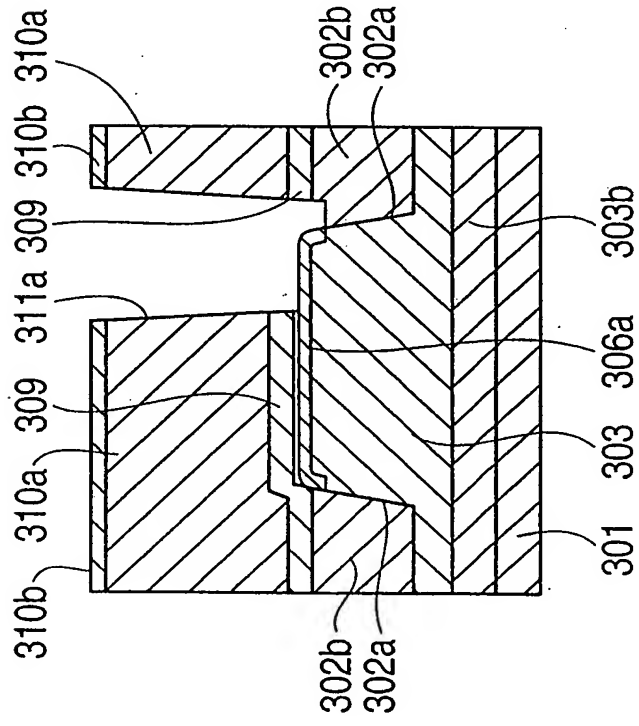
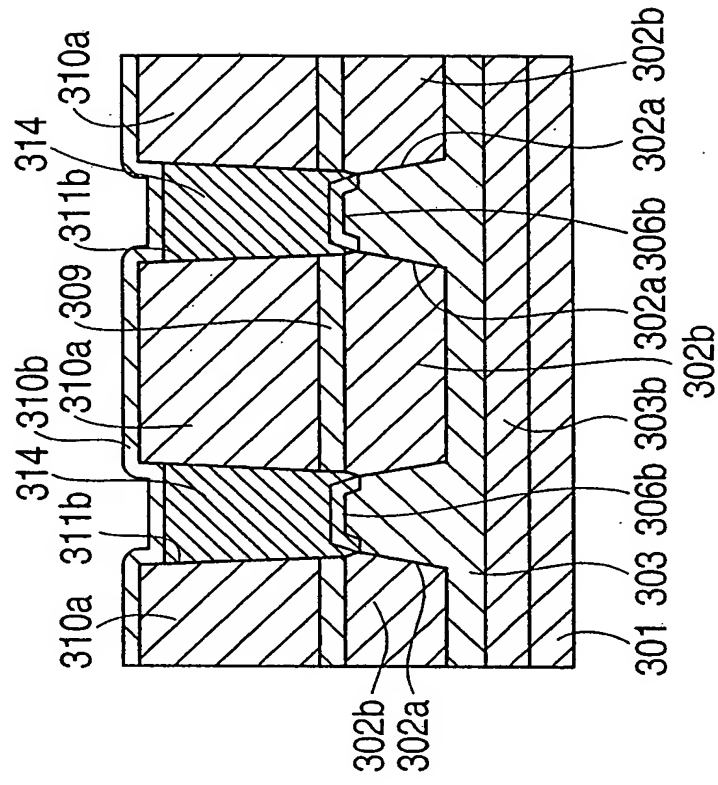


FIG. 69(b)



**FIG. 70(b)**

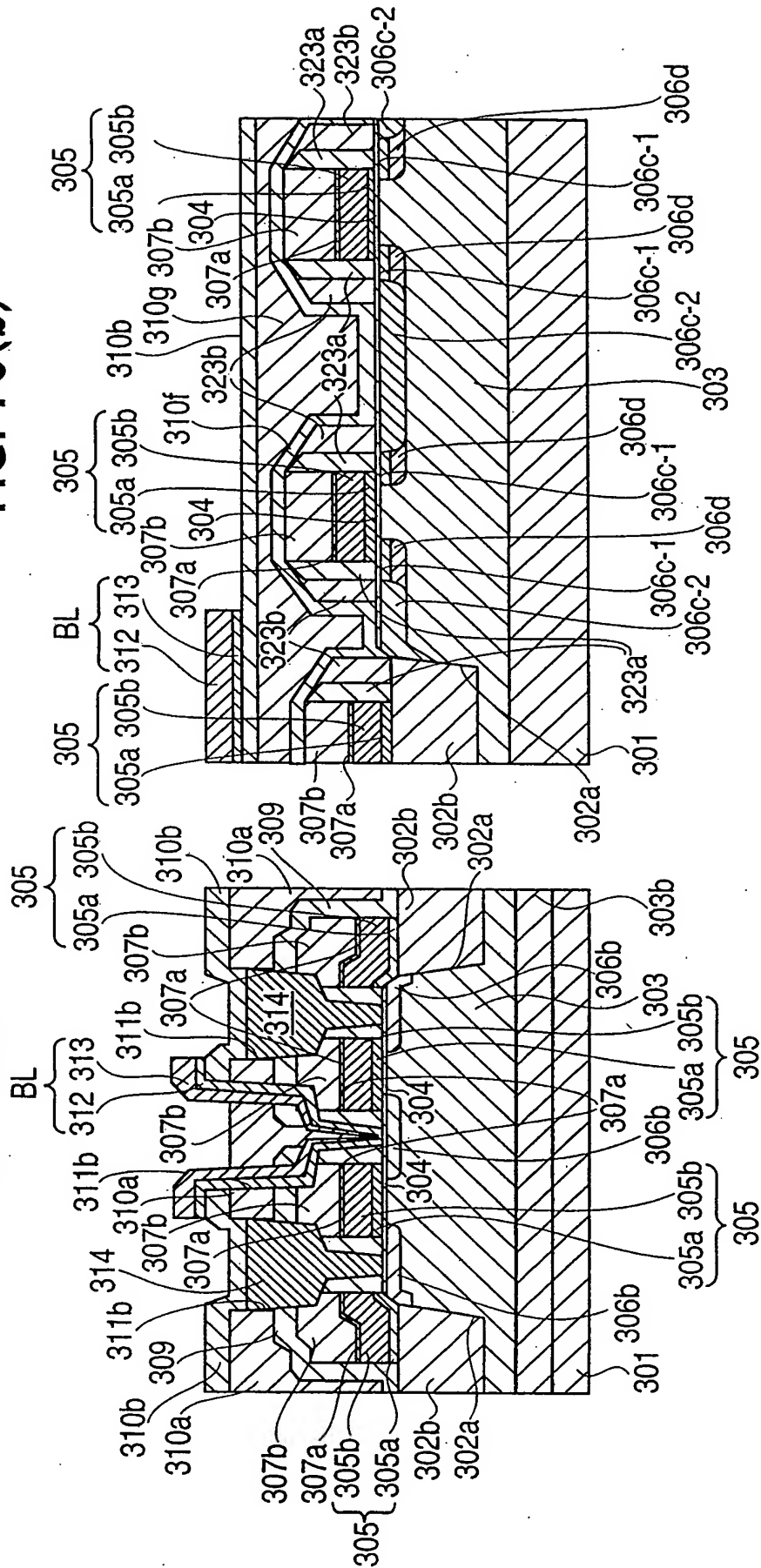


FIG. 71(a)

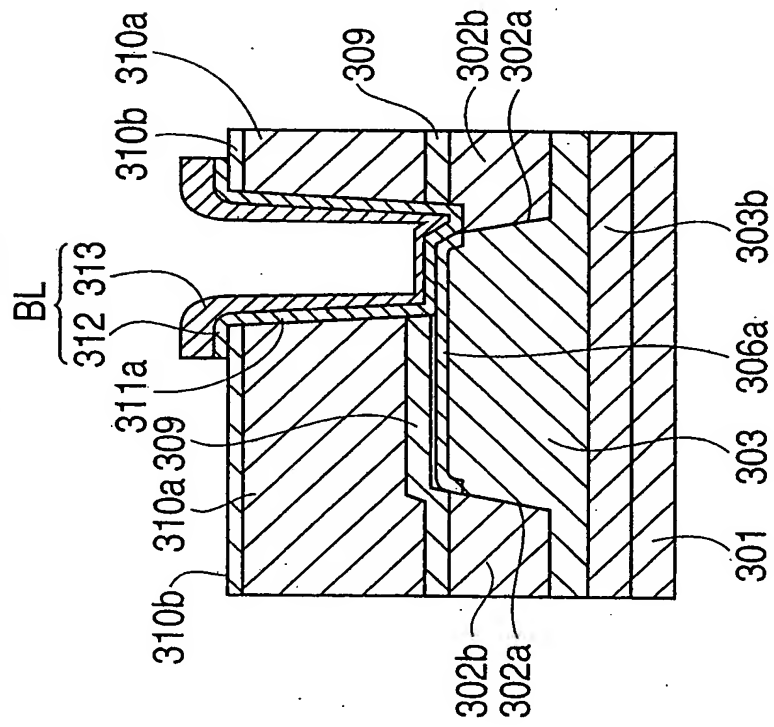
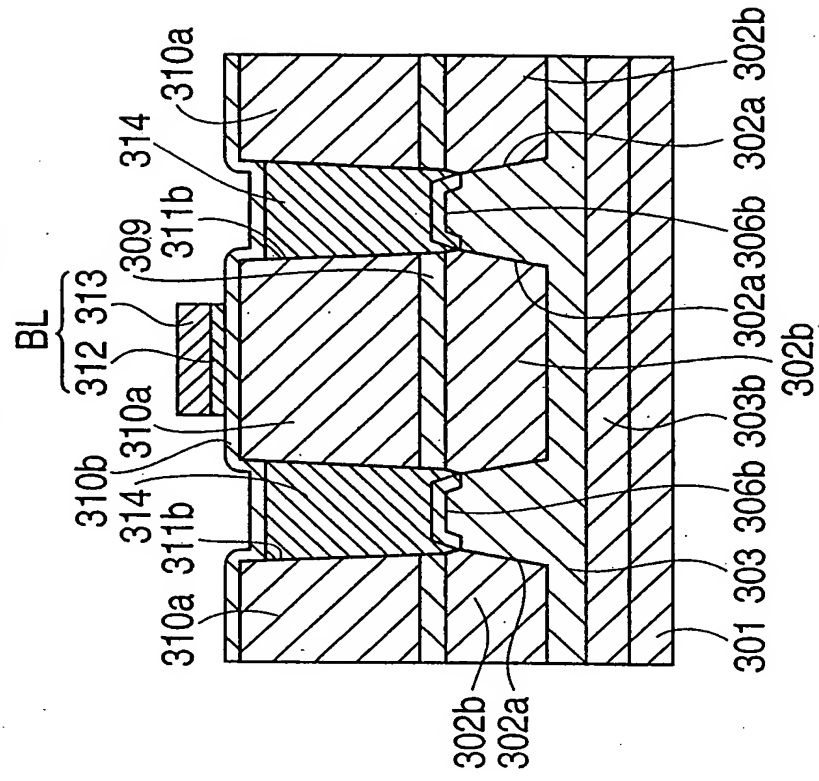
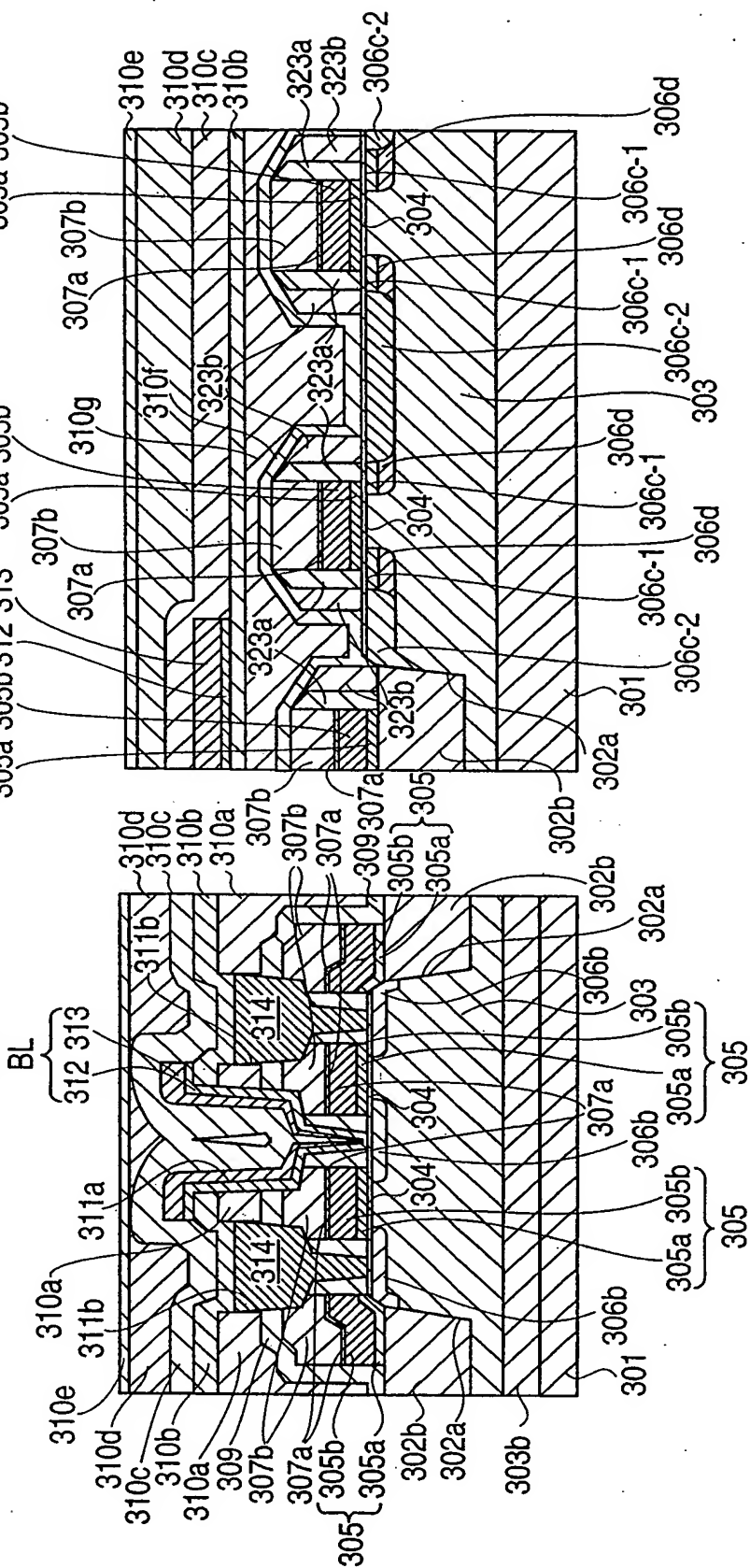


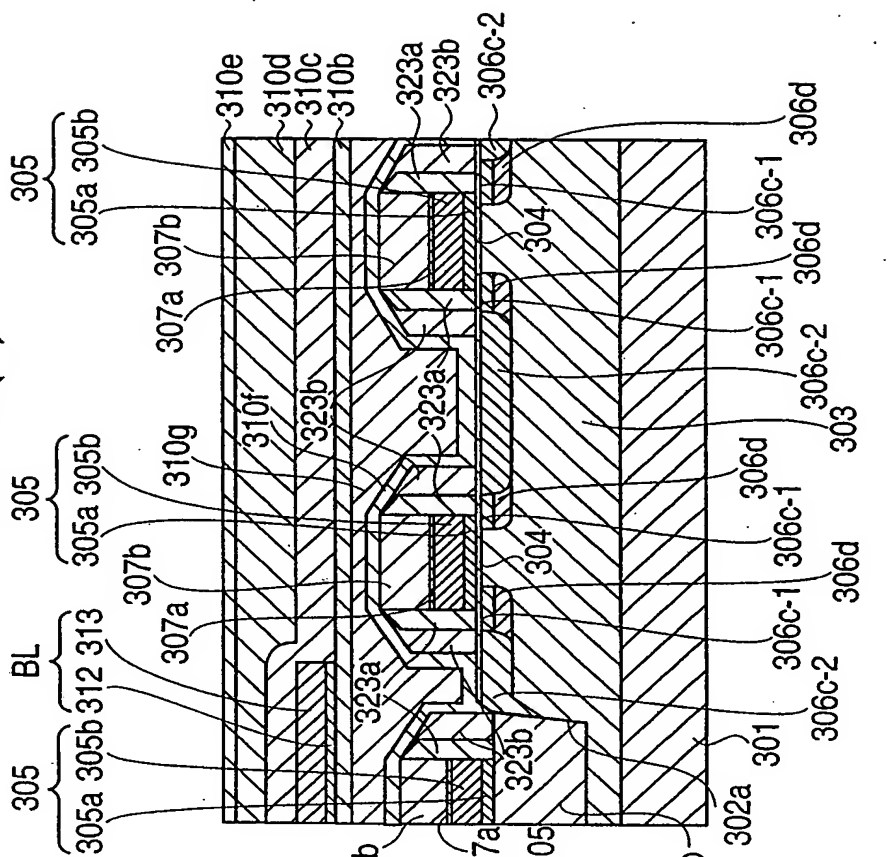
FIG. 71(a)



**FIG. 72(a)**



**FIG. 72(b)**





**FIG. 73(b)**

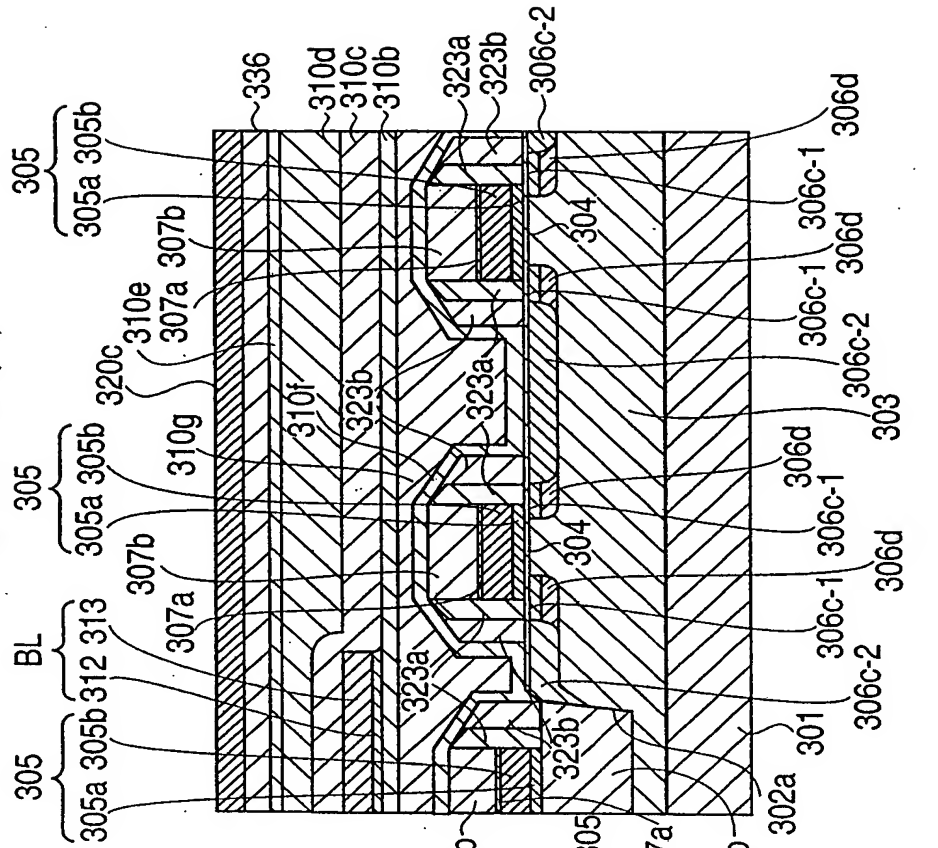


FIG. 74(a)

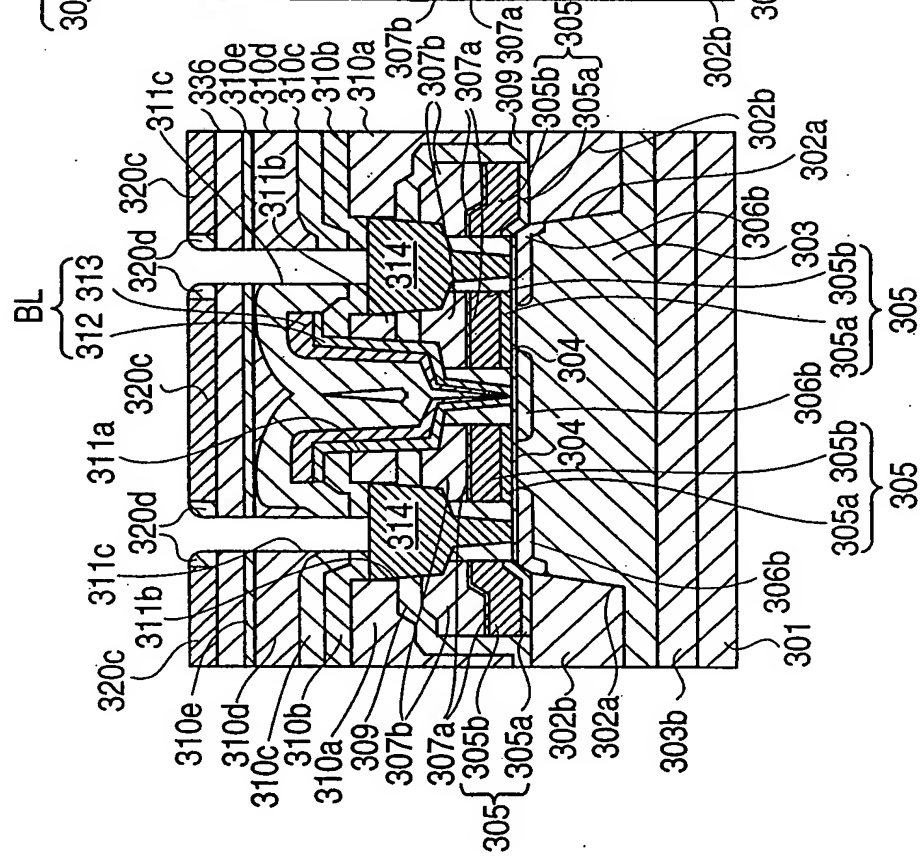


FIG. 74(b)

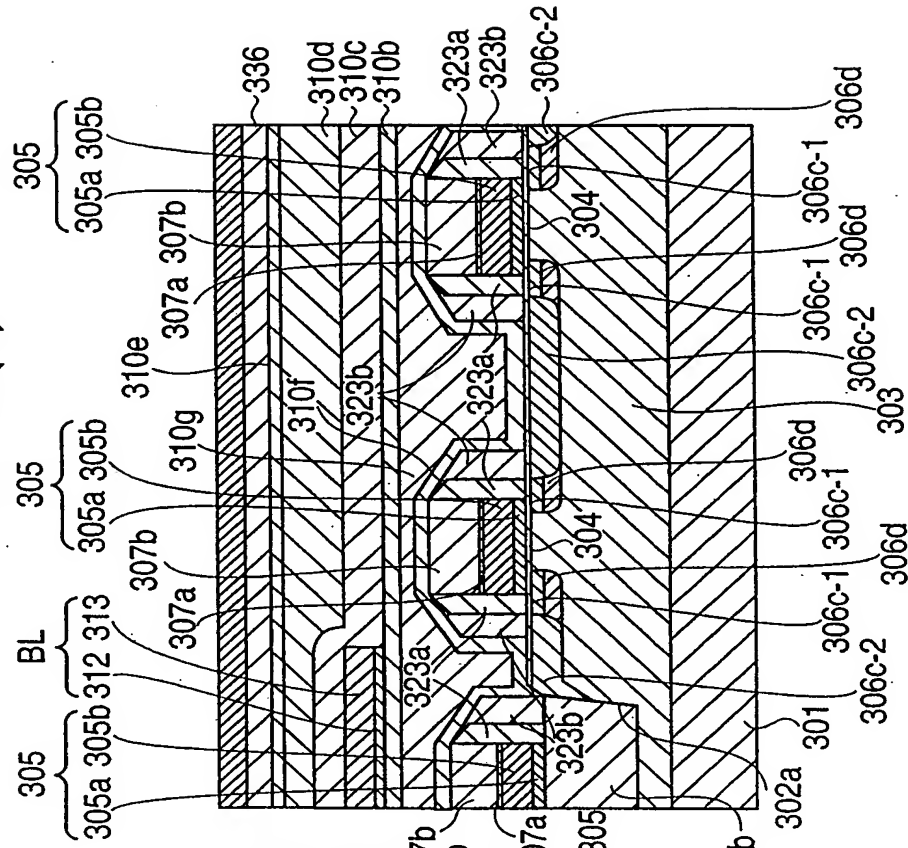


FIG. 75(a)

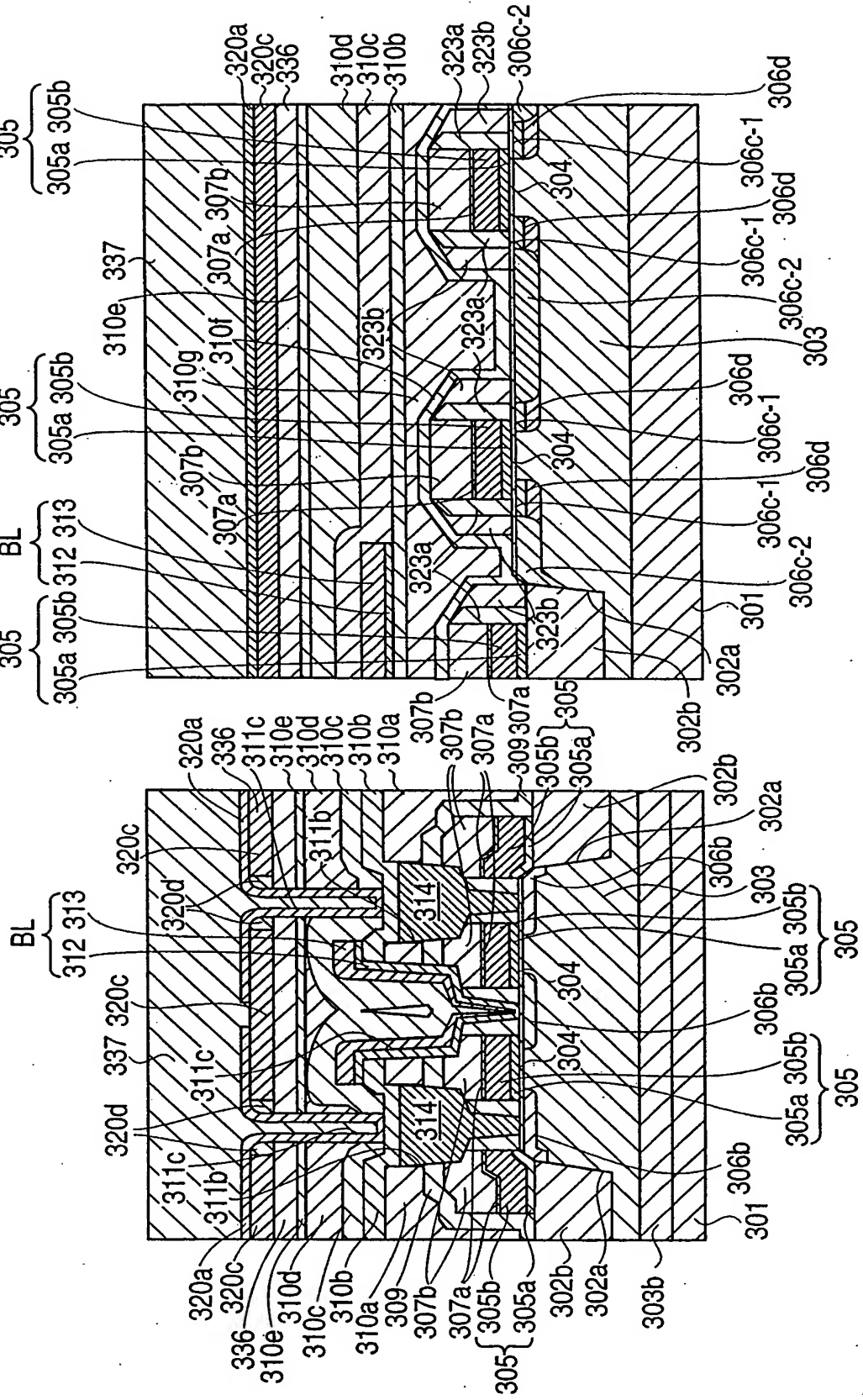
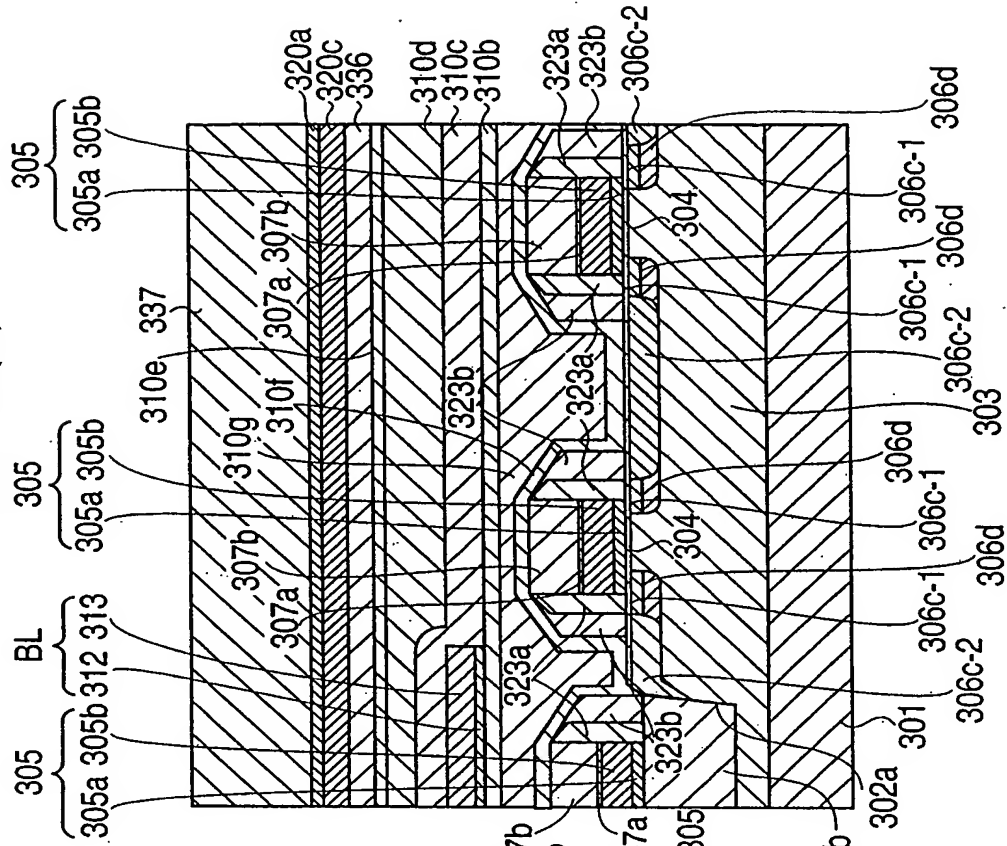


FIG. 75(b)



18



**FIG. 77(b)**

FIG. 77(b) is a cross-sectional view of a semiconductor device, similar to FIG. 77(a), showing a different internal structure. It features a substrate 301 with a top layer 302a. A series of vertical structures 305 are formed, each containing a core 310 (310a, 310b, 310c, 310d, 310e, 310f, 310g) and a surrounding layer 307 (307a, 307b). These structures are connected to a common layer 303. A top layer 306 (306a, 306b, 306c-1, 306c-2, 306d) is formed over the structures. The diagram is labeled with various reference numerals indicating different components and layers.

**FIG. 77(b)**

**FIG. 78(b)**

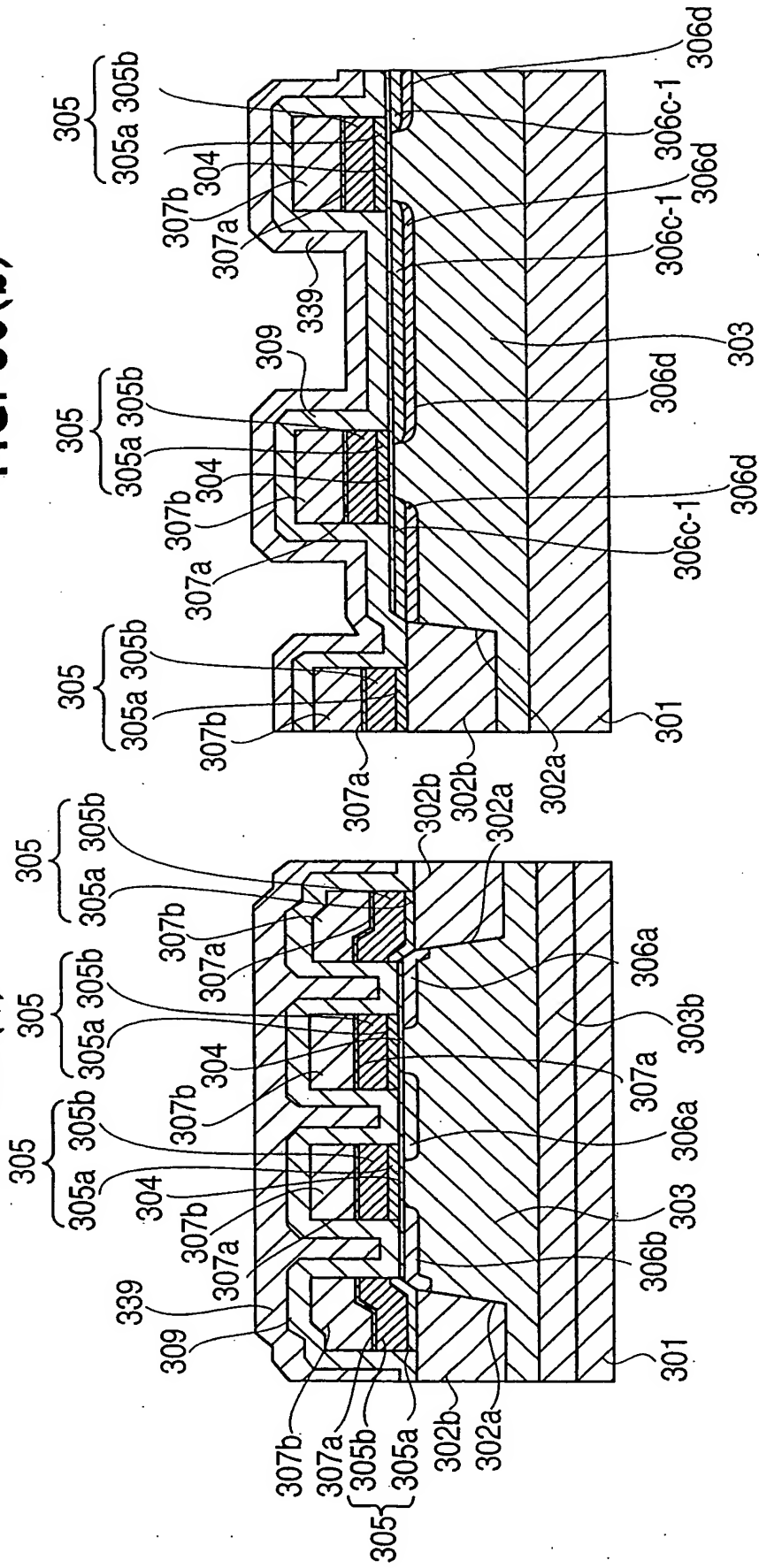
18



**FIG. 79(b)**

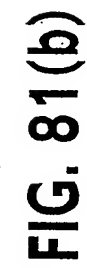


**FIG. 80(b)**

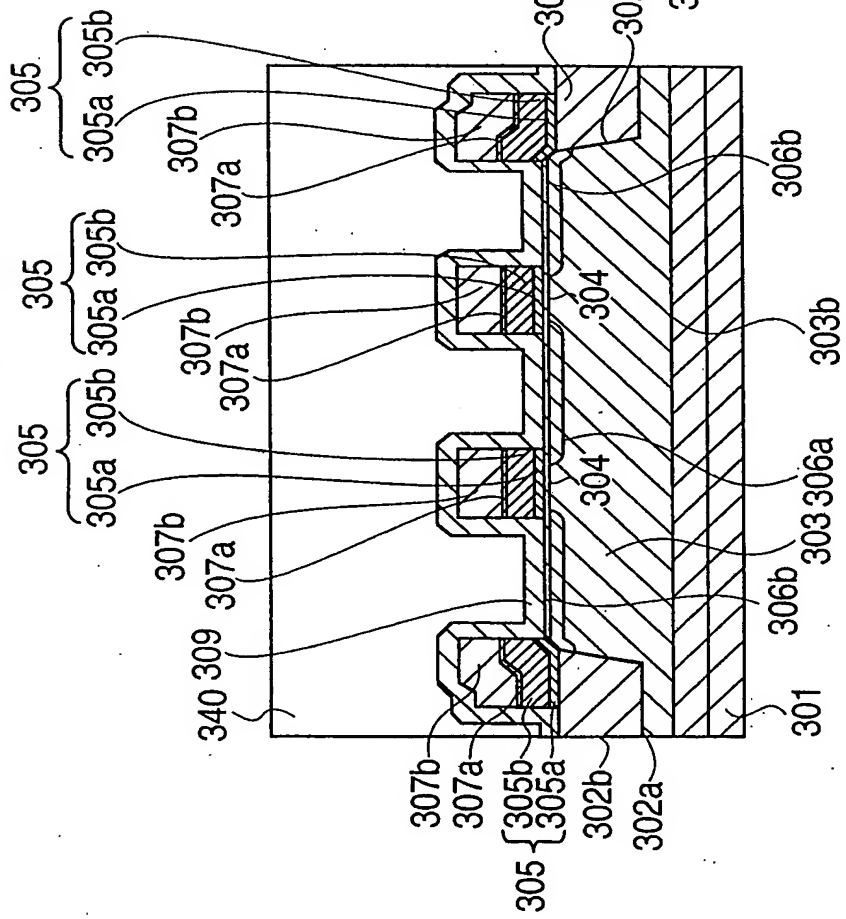




**FIG. 81(b)**



**FIG. 82(a)**



**FIG. 82(b)**

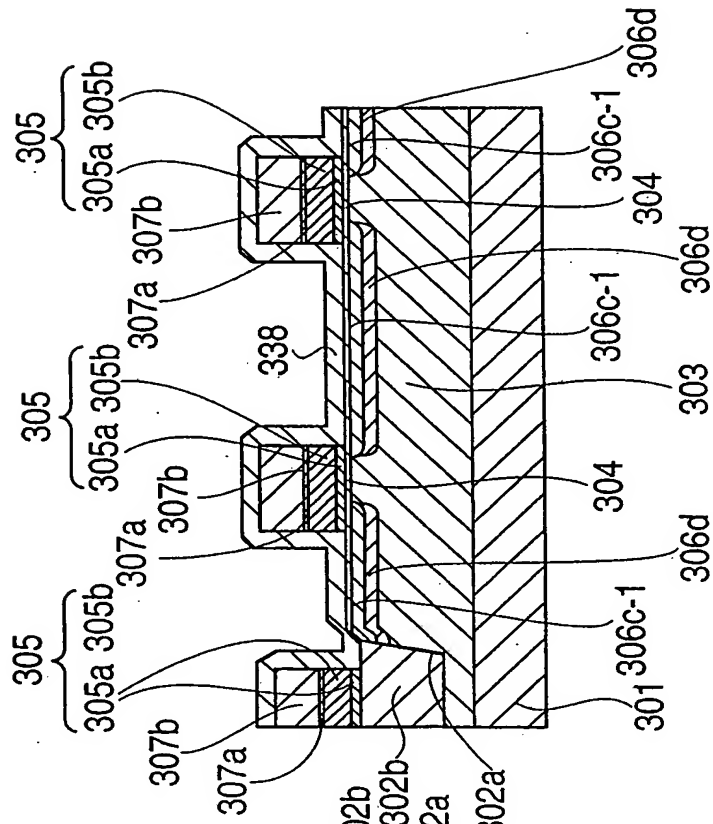


FIG. 83(a)

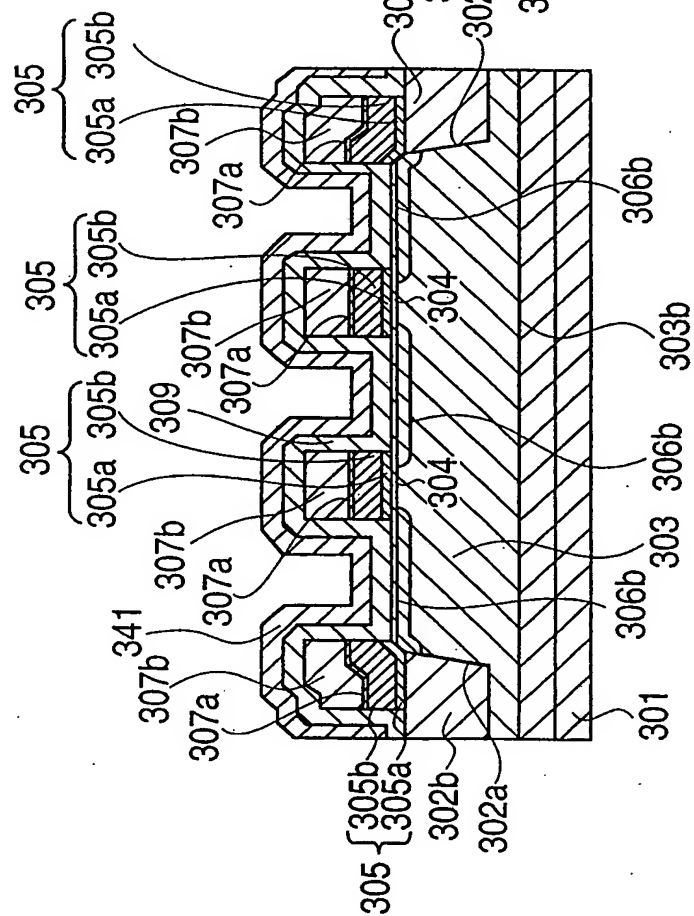
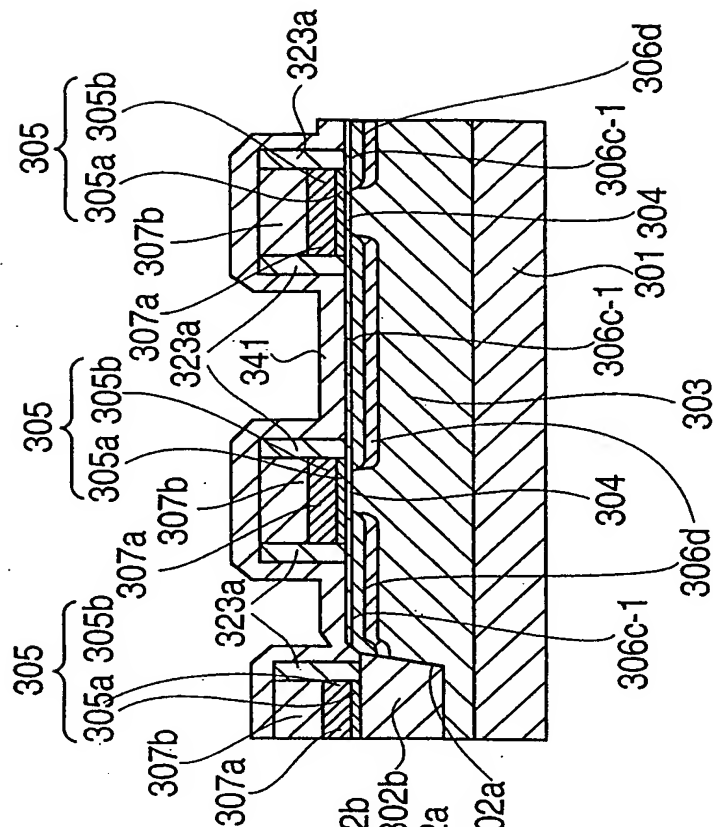
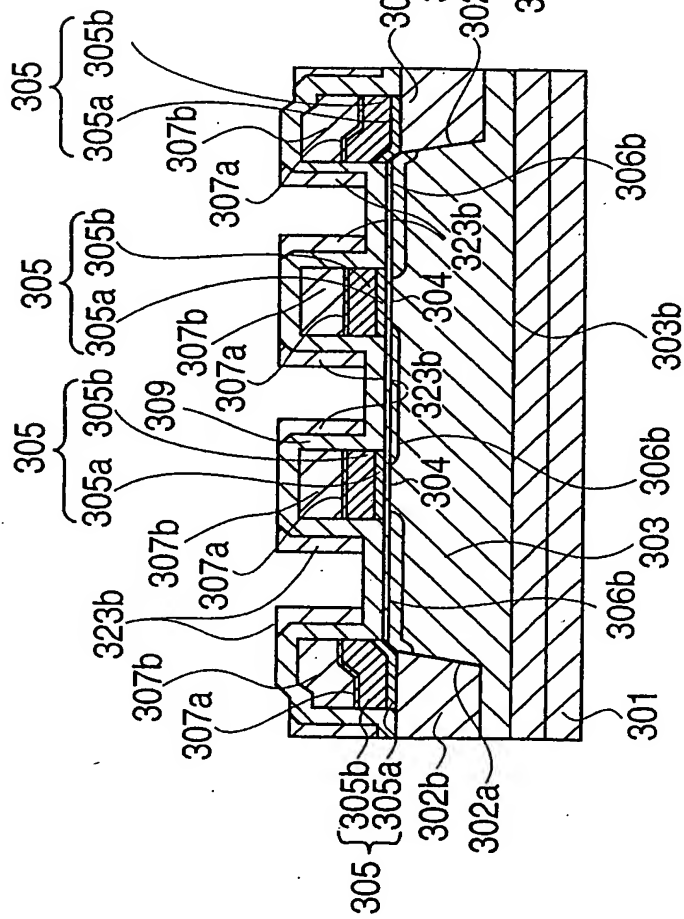


FIG. 83(b)



**FIG. 84(a)**



**FIG. 84(b)**

